# OXIDE CHARGE DEGRADATION OF MOS TRANSISTOR CURRENT AND MOBILITY IN THE LINEAR AND SATURATION RANGES

By

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The effects of charged oxide traps on the electron effective mobility (or conductivity mobility) and the linear and saturation currents in the inversion surface channel of the n-channel metal-oxide-semiconductor transistor (nMOST) are investigated. The deep $E_C$-7eV and the shallow $E_C$-1eV traps of the oxygen vacancy center in the gate oxide are charged using substrate-hot-electron injection (SHEi) and Fowler-Nordheim tunneling electron injection (FNTEi) methods and subsequently neutralized by electric field-stimulated electron (EFSE) emission or low-field SHEi. The effective mobility, $\mu_{eff}$, and saturation mobility, $\mu_{sat}$, of the electrons are monitored during charging and discharging cycles and shown to decrease because of increased Coulombic scattering in the surface channel during the charging stage, and to recover during the discharging stage. In addition, changes of the drain saturation current, $\Delta I_{D\text{-}sat}$, and gate threshold voltage, $\Delta V_{GT}$, are also monitored and the effects of $\Delta V_{GT}$

and $\Delta\mu_{sat}$ on $\Delta I_{D\text{-}sat}$ are separated. A linear dependence of the electron effective mobility, $\Delta\mu_{neff}$, on the separated positive and negative charges stored in the oxide is demonstrated for the first time.

The effects of areally nonuniform oxide charges and interface traps in the gate oxide are separated using a new procedure which combines two experimental d.c. characteristics: the subthreshold drain-current swing and the d.c. base recombination current, $I_B$. Electrons are injected into the gate oxide by areally uniform and nonuniform methods to demonstrate this new technique.

Finally a new current-accelerated channel-hot-carrier (CHC) methodology is demonstrated for rapid time-to-failure extrapolation of submicron MOSTs. This is demonstrated using the n-channel bipolar MOST (nBiMOST) test structure with $\Delta I_B$ as the monitor for the degradation. This technique gives an acceleration, or stress time reduction factor as high as 200 at the low operation drain and gate bias voltages (less than 3.3V) required in future generations of deep sub-half-micron MOSTs. This is in contrast to voltage-accelerated channel-hot-electron CHE which uses higher stress voltages (6V, 8V or higher) to elevate the kinetic energy distribution of the channel electrons and therefore changes the dominant failure mechanisms.

# CHAPTER 1
# INTRODUCTION

Since the initial theoretical work on the carrier mobility in the semiconductor surface inversion layer by Schrieffer [1,2] and the channel conductance measurements of Brown and Kingston [3,4], mobility studies have been made extensively using the metal-oxide-semiconductor field-effect transistor (MOST or MOSFET). Characterization of the carrier mobility is essential for advancing today's deep submicron ULSI (Ultra large scale integrated) circuit technology to manufacture multi-million-transistor chips since it is directly proportional to the MOST's output current to charge up the load capacitance which limits the clock frequency of digital ULSI circuits and since it is also directly proportional to the MOST's transconductance and the cutoff frequency which limits the bandwidth of analog ULSI circuits. Accurate wide-range characterization of the carrier mobility requires an in-depth quantitative understanding of the physical scattering mechanisms which limit the mobility in the MOST channel. The physics-based understanding is essential to the development of accurate MOST device simulators that do not rely solely on calibrations using experimental data that cannot assure accurate mobility extrapolation outside of the mobility calibration range.

As the complementary-MOS (CMOS) and bipolar-CMOS (BiCMOS) integrated circuit technologies continue to scale down the gate oxide thickness (below 50Å), and

the channel lengths (below 0.1μm) [5-8], the impurity dopant concentrations in the CMOS wells and the MOST channels have to be increased accordingly to minimize the various short-channel effects which give undesirable MOST characteristics. The electric field also increases as the dimension decreases. The higher electric field and dopant impurity concentration confine the inversion layer charge closer to the interface, causing a higher carrier scattering rate due to the proximity of the carriers to the atomically rough oxide/silicon interface and the charges in the gate oxide. The higher electric field also increases the electric instability of the gate oxide via electron and hole trapping at the existing and stress-generated oxide traps and at the stress-generated oxide/silicon interface traps. Furthermore, the higher transistor density from smaller transistor dimensions would raise the operation temperature of the transistors and the ULSI circuit chips. Thus, the three major mobility reduction factors are the higher longitudinal and transverse electric fields, the confinement of the charge carriers (electrons or holes) near the oxide/silicon interface, and higher operation temperatures.

The effects of trapped charges in the silicon substrate, gate oxide layer, and polysilicon (poly) gate, and at the poly-gate/$SiO_2$ and $SiO_2$/Si-substrate interfaces on MOST characteristics have been studied by numerous investigators and reported in the literature [9]. The magnitude, sign, and distribution of these trapped charges, in relation to the conduction carriers (electrons or holes) in the surface channel, can alter the threshold voltage, $V_{GT}$, and the channel effective mobility, both of which govern the shape of MOST's drain current-voltage ($I_D$-$V_D$) characteristics. So far, studies on the effects of these charges on the carrier mobility have been limited to carrier scattering by the charged Si/$SiO_2$ interface traps and ionized impurity centers in the Si

substrate, and the Coulombic screening of the charged traps by the large carrier density in the surface inversion channel.

In general, confinement of the inversion carriers closer to the interface will increase surface (atomic) roughness scattering and convert phonon scattering from the three-dimensional (3-d) to the more effective 2-d 'surfons' scattering as the quantum energy states in the potential well of the surface channel become quantized [10, p.668]. Furthermore, there will be increased Coulombic scattering from the charges in the poly-gate and the oxide and interfacial layers mentioned above because of the closer proximity of these charges to the carriers in the conducting channel. Carrier confinement will reduce scattering from ionized bulk impurities unless there is a corresponding increase in the impurity concentration; higher impurity concentration is frequently used to suppress short channel effects in recent generations of submicron MOSTs. The higher MOST operation temperature from higher dc power density will also increase phonon scattering and reduce the coulombic scattering.

There have been two effective mobilities measured and theorized for the surface channel and the MOS transistors. The first effective mobility is obtained from the MOST's channel conductance measurements in the linear channel current-voltage range, given by the drain conductance, $g_d=\partial I_D/\partial V_D$ with $V_G$=constant, in the linear MOST drain current-voltage ($I_D$-$V_D$) range. This will be denoted by $\mu_c$, $\mu_{linear}$ or $\mu_{lin}$.

The second effective mobility is obtained from the MOST's transconductance measurements, $g_m=\partial I_D/\partial V_G$ with $V_D$=constant, which will be denoted by $\mu_{gm}$. This experimental mobility is highly dependent on the energy and spatial distribution of the

interface traps at the oxide/silicon interface. Thus, it is difficult to obtain reliable results from an analysis of the experimental data.

The third effective mobility is obtained from least-squares-fit of the experimental saturation drain current versus gate voltage data ($I_{D\text{-}sat}$-$V_G$) to the analytical equation based on the simple bulk-charge theory. This mobility will be denoted by $\mu_{sat}$.

Two effective mobilities are measured and compared with theory in this thesis: the linear and saturation mobilities, $\mu_{lin}$ and $\mu_{sat}$. The linear mobility provides the most direct experimental evaluation of the various scattering mechanisms which reduce the mobility. The saturation mobility gives the transistor parameter that goes into the transistor model used in the circuit analysis of MOS ULSI circuits.

In this thesis the effects of charge trapping and detrapping, in the gate oxide layer, on the two effective mobilities are studied. Variation of the drain current due to controlled changes of oxide charge density will be correlated individually to $\Delta V_{GT}$ and $\Delta\mu_{sat}$. This gives the effects of Coulombic scattering of the channel electrons by the positive and negative charges in the gate oxide on mobility. All measurements were undertaken using the n-channel bipolar-MOST (n-BiMOST) test structure, therefore, the scope of this thesis is limited to the study of electron effective mobilities in the surface channel. Nevertheless, the new fundamental understanding and new experimental methodologies are also applicable to hole mobilities in silicon p-channel MOSTs.

Results of detailed studies are described in this thesis on the variation of the mobilities ($\mu_{lin}$ and $\mu_{sat}$), gate threshold voltage $V_{GT}$, and drain saturation current, $I_{D\text{-}sat}$, caused by the three charge states (-1, 0, +1) of the bridging oxygen vacancy in the gate

oxide. The oxygen vacancy was also known as the E' center delineated prior to 1979 by electron paramagnetic resonance experiments. The oxygen vacancy was charged and discharged or neutralized by Fowler-Nordheim tunneling electron injection (FNTEi), substrate hot electron injection (SHEi), and Fowler-Nordheim tunnelling electron emission (FNTEe) techniques, while the MOST's $I_D$-$V_G$ and $I_D$-$V_D$ characteristics are monitored. Koomen's [11] split-CV method was used to measure the carrier capacitance in the inversion surface channel, $C_{inv}$, which was then used to calculate the inversion carrier charge density, $Q_{INV}$. The linear mobility was then computed from $\mu_{lin} = g_d/(W/L)Q_{INV}$ where W/L is the channel width to length ratio or the aspect ratio. The linear $I_D$-$V_G$ (at three constant $V_D$: $V_{D1}$, $V_{D2}$, and $V_{D3}$) and the saturation $I_{D\text{-}sat}$-$V_{D\text{-}sat}$ ($V_D = V_G = V_{Power\text{-}supply} \geq V_G - V_{GT} \simeq V_{D\text{-}sat}$) were measured before and after each electron injection-capture/emission cycle which gave the $V_{GT}$, $I_{D\text{-}sat}$, $\mu_{sat}$ and $\mu_{lin}$ as a function of the charged oxygen vacancy center.

The second part of this research concerned the effects of nonuniform charging of the gate oxide using channel-hot-electron (CHE) and substrate-hot-electron (SHE) injection to stress the n-channel MOS transistor. A new technique is demonstrated for separating the effects of uniform or nonuniform interface traps and nonuniform oxide traps along the length of the MOST channel. The technique makes use of the recently developed direct-current current-voltage (DCIV) method [12] to monitor interface trap generation, and the well-known change of the subthreshold drain-current swing, $\Delta S$, to monitor the spatial uniformity of the trapped oxide charge during the controlled oxide trap (oxygen vacancy) charging and discharging cycles. In addition, the recently demonstrated current-acceleration methodology for rapid time-to-failure measurement

in bipolar junction transistors (BJT), proposed by Neugroschel and Sah [13], is extended for the first time to MOS transistors under CHE stress. This new MOST acceleration stress technique makes use of the BiMOST's unique vertical BJT bottom-emitter junction to accelerate the time-to-failure while maintaining the same drain and gate voltages ($V_D$, $V_G$), which determine the kinetic energy and distribution of the injected carriers. This new MOST acceleration stress technique is further extended to regular MOSTs which do not have a substrate junction emitter by forward biasing the source junction as proposed by Sah. The three failure parameters measured are the increasing base current measured by the DCIV method, the change in the gate threshold voltage, and the change in the drain saturation current.

Chapter 2 will review the scattering mechanisms affecting the carrier mobility in the surface inversion layer of MOS transistors. The measurement setup and BiMOS transistor fabrication and operation details will be described in chapter 3. The effects of charged oxide traps on the mobility, saturation current, and threshold voltage are discussed in chapter 4. Experiments demonstrating a new measurement technique for the separation of interface traps and areal oxide charge nonuniformity will be presented in chapter 5. Finally, the two new current-accelerated channel hot electron stress methodologies are presented in chapter 6 which forward bias the substrate or source n/p junction emitter to increase the channel hot electron current.

# CHAPTER 2
# SURFACE INVERSION CARRIER TRANSPORT THEORY

The three primary scattering mechanisms which contribute to the inversion carrier mobility degradation as reviewed by Sah and his graduate students [14-16] included the following: 1) lattice scattering due to acoustical and optical phonons, 2) Coulombic scattering due to ions and dipoles in the oxide and at the $SiO_2$/Si interface, and impurities in the silicon surface space-charge layer, and 3) surface roughness scattering due to the interfacial atomic irregularities. One must also consider Coulombic screening by the inversion-layer carriers and the effective mass anisotropy in 2-d conduction due to 1-d quantization in the surface channel's quantum well from the high transverse electric field. These scattering mechanisms will be reviewed in this chapter based on the theoretical analyses given by the previous investigators as reviewed by Sah [14-16].

## 2.1 Theoretical Calculation of $\mu$

The general theory of inversion layer transport and carrier effective mobility was first presented by Schrieffer [1] to account for the reduced conductivity due to diffuse surface scattering. Diffuse scattering refers to the assumption that the probability of scattering is equal in every direction. Schrieffer solves the Boltzmann transport

equation using the relaxation time approximation to obtain the inversion carrier distribution function,

$$f = f_0 + f_1(v,z) \tag{2.1}$$

where $f_1$ represents a small perturbation to the equilibrium Boltzmann distribution function, $f_0$. Using a random scattering boundary condition to eliminate $f_1$ at the interface, (x=0), the current density is found by integrating $f_1$ in the velocity space,

$$i_y = q\int dv_x dv_y dv_z \, v_y f_1 \tag{2.2}$$

Here $v_y$ and $v_z$ are the carrier velocities parallel to the interface and $\hat{x}$ is the normal (or transverse direction) to the interface. By integrating the current density from the interface to the edge of the inversion layer, $x_i$, one finds the total d.c. current, $I_Y$, due to a constant longitudinal field $E_Y$. The conductivity effective mobility or linear mobility is then defined as,

$$I_Y = q\mu_{lin} N_{INV} E_Y. \tag{2.3}$$

The inversion carrier density, $N_{INV}$, is calculated for an assumed triangular potential well (constant transverse field, $E_X$),

$$E_X = d\Phi/dx = \text{constant} \tag{2.4}$$

$$\nabla^2\Phi = \rho/\varepsilon_s \tag{2.5}$$

or by solving the Poisson equation for the potential well profile at the silicon surface.

## 2.2 Surface Quantization

Schrieffer at the suggestion of Bardeen [2] also recognized the possibility of 1-d or transverse quantization at high transverse fields $E_X$ near the silicon surface. As the

applied d.c. gate voltage increases the surface energy band bending, the potential well at the silicon surface becomes narrower and deeper; eventually quantizes the motion in the x-direction giving quantized (discrete) energy subbands perpendicular to the surface. This restricts inversion carrier motion to the two dimensions, y and z, parallel to the interface within each 2-d energy subband. The two-dimensional transport in the surface inversion layer was first observed by Fang and Fowler [17,18] using magnetoconductance measurements on a <100> silicon surface at low temperatures. Stern, Howard and Fang [17-20] performed selfconsistent calculations of the Schroedinger and Poisson equations to illustrate the energy splitting between the ground and the first excited 2-d energy subbands. Calculations were made using the variational approach with the assumption that all the carriers occupy the lowest energy subband and that the potential is a function of x only. The boundary conditions assumed were as follows: (i) the potential vanishes at $x=\infty$, (ii) the transverse field, $d\Phi/dx$, vanishes at the interface (x=0), and (iii) the electron wave function $\Psi$ vanishes at the interface (infinite $SiO_2$/Si barrier height or zero penetration into the oxide) and deep in the bulk silicon ($x=\infty$). The envelope function, $\xi(z)$, of the electron wave function

$$\Psi = \xi(z)\exp(ik_1x + ik_2y) \tag{2.6}$$

is then

$$\xi(z) = \zeta(z)\exp[-iz(W_{13}k_1 + W_{23}k_2)/W_{33}] \tag{2.7}$$

where $\zeta(z)$ are the eigenfunction solutions of the Schroedinger equation and $W_{ij}$ is the reciprocal effective mass tensor (1-x, 2-y, 3-z). Solving the wave equation, they compute the energy eigenvalues and an average distance from the interface for

inversion carriers in the channel. Their results illustrate the dependence of the quantized energy splitting on well doping concentration, temperature, transverse field in the silicon, $E_X$, and crystal orientation.

Subsequent theoretical work by Pierret and Sah [21] supported the strong variation in effective mobility with well doping concentration in weak inversion near $V_{GT}$ (when the surface potential, $\Phi_S$, equals twice the bulk potential $\Phi_S=2\Phi_F$). They also noticed that the effective mobility approached a common value versus doping at higher transverse fields or as the inversion charge density became degenerate.

## 2.3 Crystalographic Anisotropy

In the surface inversion layer the silicon crystal's cubic symmetry is disrupted by the transition into the $SiO_2$ layer and hence one must also refine the isotropic bulk mobility theory to include the crystal orientation dependence. The first theoretical treatments were presented by Ham and Mattis [22] assuming a constant surface field and using a special set of spatial transforms to convert the ellipsoidal energy surfaces to spherical ones. Their constant transverse field, $E_X$, (or triangular potential well) assumption was removed by Pierret and Sah [21] who gave the solutions for the exact electric field which used the Boltzmann transport equation and considered the distribution function, f, for each of the six ellipsoidal conduction valleys in E-k space. The analysis was then converted from k-space to velocity space (v-space) using the spherical relation for the velocity,

$$v_x = (1/\hbar)dE/dk \qquad (2.8)$$

while the appropriate mass tensor is substituted for the spherical effective mass, $m^*$. Pierret and Sah also assumed that the surface inversion layer is nondegenerate, there is no intervalley scattering, and a constant relaxation time may be used. The key difference in this solution compared to the isotropic case is that the inversion carrier velocity in the longitudinal direction, $v_y$, is now dependent on the transverse velocity, $v_x$. Fortunately, however, if the normal to the interface is in the <100> direction, $v_x$ is once again decoupled from the carrier velocity parallel to the interface and conduction becomes isotropic. Since the samples tested in the present study are oriented in the <100> direction, as is the case in most of today's and future MOST technologies, the effects from anisotropic conduction will not be included in this thesis.

## 2.4 Screened Coulombic Scattering

As discussed earlier, the sources of Coulombic scattering include 1) ionized impurities in the surface space charge layer of the silicon substrate and the polysilicon gate, 2) charges in the gate oxide, and 3) isolated or dipole type charges located at the polysilicon- gate/oxide and oxide/silicon-substrate interfaces. The key parameters governing this form of scattering are 1) Coulombic screening by the mobile inversion charge in the channel, 2) the distribution of these mobile charges within the surface space-charge layer in the silicon, 3) the proximity or distribution of all the Coulombic scattering sources with respect to the inversion layer, and 4) the position correlation of the scatterers or the degree of randomness in their spatial distribution. The general problem for calculating mobility involves finding the change in potential energy of the

inversion carriers in the presence of these scattering centers. For example, if a scatterer lowers the potential energy, then the carrier density increases in the vicinity of this scatterer while the reverse is true for a decreased potential. Hence the mobile charge redistributes itself so that the scattering center's potential is screened.

Greene and O'Donnel [23] first considered the problem of scattering in the presence of surface charges. They calculated the surface reflectivity in terms of the differential scattering probability for a shielded Coulombic potential of N randomly placed surface charges. Stern and Howard [19] also reformulated their analysis for the lowest energy subband in the quantized surface to account for the additional screened Coulombic potential due to ionized impurities in the silicon depletion layer as well as any oxide and $Si/SiO_2$ interface charges. Using first order perturbation theory, their assumed potential, $\bar{\Phi}(r)$, which varies with $r=(y^2+z^2)^{1/2}$ and x, induces a change in the $i^{th}$ eigenvalue $\delta E_i(r)$ of the mobile inversion charge,

$$\delta E_i(r) = -q\bar{\Phi}(r) = -q\int \delta\Phi(r,x) g_i(x)\, dx \tag{2.9}$$

$$g_i(x) = (1/2)b^3x^2\exp(-bx) = |\zeta_i(x)|^2 \tag{2.10}$$

$$b = \{[48\pi q^2 m_3/\varepsilon_s\hbar][N_{DEP} + (11/32)N_{INV}]\}^{1/3}. \tag{2.11}$$

where $g_i(x)$ and $\zeta_i(x)$ are the charge distribution function and the normalized eigenfunction for the Stern and Howard 2-d ground state subband [19]. The induced charge density in the inversion layer, $\rho_{ind}$, is expressed in terms of the reciprocal screening length $s_i$,

$$\rho_{ind}(r,x) = -(\varepsilon_s/2\pi)q\Sigma_i\, s_i\, \Phi_i(r)\, g_i(x). \tag{2.12}$$

Ning and Sah [24] extend this single ion formulation by solving Poisson's equation for $\delta\Phi$ due to a distribution of oxide charge at $r_n$ locations in a plane within the oxide,

$$\nabla^2\delta\Phi(r,z) - 2s\Phi(r)g(z) = (4\pi/\varepsilon_s)q\Sigma\delta(r-r_n)\delta(z) \qquad (2.13).$$

$N_{ox}A$ is the total number of oxide charges in a sheet of area A with an oxide charge areal density $N_{ox}$. Once the potential fluctuation $\Phi(r)$ is known, the scattering transition rate, $\Gamma_{kk'}$, is found using the 'golden rule' and the Stern and Howard [19] 2-d ground state plane wave, $\Psi$,

$$\Gamma_{kk'} = 2\pi/\hbar <|<\Psi_{k'}|(-q\delta\Phi)|\Psi_k>|^2>_{ave}. \qquad (2.14)$$

The inversion layer mobility, $\mu$, may then be found numerically or by using the Born approximation to calculate $\Gamma_{kk'}$,

$$\mu = (q/m_c)\int y\tau(f_o - 1)dy/\int f_o dy \qquad (2.15)$$

$$\tau = \Sigma\Gamma_{kk'}(1 - \cos\Theta). \qquad (2.16)$$

Stern and Howard [19] illustrate the use of the Born approximation for a single ionized impurity located at $x=x_o$ and discuss the validity of this approximation in great detail by comparison with numerical phase-shift calculations. The approximation is inaccurate at extremely low temperatures, or high doping impurity concentrations or other scattering charge densities. This stems from the first order perturbation analysis used in this approximation which assumes the 2-d wave function, $\Psi$, is unchanged in the presence of the charged scatterers. Other sources of error found in this analysis include the assumptions of a spherical effective mass, the neglect of screening by inversion carriers and the possibility of conduction in higher energy subbands at higher transverse fields, temperatures and inversion carrier densities. Furthermore, the average distance between the inversion layer and the surface charge scattering centers was shown to have a pronounced effect on the mobility as would be expected from the 1/r dependent Coulombic potential.

The subject of the charged scatterer's spatial distribution and the effects of position correlation of the scatterer were treated by Ning and Sah [24, 25]. These authors reformulate the scattering problem into a simpler 2-d case where the potential perturbation arises from the spatial variations in the local charge density. The charge density fluctuations $\delta\rho$ are represented as,

$$\delta\rho(r) = \rho(r) - \rho^{o}(x) \tag{2.17}$$

$$\rho^{o}(x) = <\rho(r)>_{ave} \tag{2.18}$$

where $\rho^{o}(x)$ represents the x spatial dependence of $\rho(r)$ averaged over the y-z plane. If the thermal wavelength of the inversion carriers, $\lambda_{th}$, is much larger than the inversion layer thickness, $x_i$, then the inversion layer can be treated as a 2-d gas. Under these conditions the perturbation analysis proceeds as before to solve for the scattering transition rate and mobility. Three sample oxide and inversion charge distributions, with or without the effects of screening and correlation were analyzed [24] and used to analyze the data [25, 26]. Their results indicate that increased correlation and/or screening by the inversion charge would increase the channel mobility.

The carrier scattering by neutral dipoles formed by the hydrogen passivation of ionized surface states at the $Si/SiO_2$ interface as first suggested by Sah also falls under the analysis discussed here. This dipole scattering rate was derived by Hess and Sah [27] using the aforementioned Born approximation. Their results indicate a $T^{1.5}$ dependence in the mobility for $T>100^{\circ}K$,

$$\mu_{DP} = \mu_o T^{1.5}/(N_{DP} L_{DP}^{2}) \tag{2.19}$$

where $N_{DP}$ is the density of dipoles at the interface and $L_{DP}$ is the effective spatial separation of the positive and negative charges in each dipole.

## 2.5 Phonon Scattering

As the temperature of the semiconductor increases, scattering due to quantized lattice vibrations, or phonons, will naturally increase. These lattice vibrations are commonly categorized as acoustical, for those with lower energies, and optical (or intervalley) for higher energies. The first theoretical analysis for surface acoustical phonon scattering by Kawaji [28] was essentially a 2-d version of the Bardeen-Shockley deformation potential theory for bulk semiconductors. In this analysis a change in potential (assumed to be an inverted triangular well) at the $Si/SiO_2$ interface originates from longitudinal phonons whose wave vectors are confined to the 2-d plane parallel to the interface. Hence these phonons only interact with inversion carriers moving parallel to the interface. The lattice displacement, $\delta R(R_n)$, in a direction $l_k$ and the corresponding dilation, $\Delta(r)$, due to a lattice wave in the 2-d surface plane are given by,

$$\delta R(R_n) = N_2^{-1/2}\, l_k\, [a_k \exp(ikR_n) + a_k^* \exp(-ikR_n)] \tag{2.20}$$

$$\Delta(r) = \nabla \cdot \delta R(R_n). \tag{2.21}$$

There are $N_2$ vibrating lattice points, and L represents the number of atomic layers in the conducting surface. The semiconductor density, $\rho$, and the mass per unit area, M, in the surface inversion layer of thickness 'd' are then related as $\rho = MLN_2$. The 2-d deformation potential is given by, $\Delta(r)E_2$, where $E_2$ is the deformation potential constant which was obtained by fitting the theory to experimental mobility data. This

potential may now be used to calculate the scattering transition matrix element, $M_{pp'}$, between the quantized 2-d inversion carrier momentum states p and p',

$$M_{pp'} = \int \Psi_{\|}(p)\Delta(r)E_2\Psi_{\|}(p')d\sigma \quad (2.22)$$

$$p = p' \pm k \quad (2.23)$$

$$\tau^{-1} = \int M^2(1 - \cos\Theta)\nu_2 d\lambda \quad (2.24)$$

The relaxation time, $\tau$, refers to the electrons traveling parallel to the interface with wave functions $\Psi_{\|}$ and $\Psi^*_{\|}$ where $\nu_2$ is the 2-d density of states along a constant energy curve, $\lambda$, in E-k space. Assuming a constant velocity, $c_{l2}$, for the 2-d phonon wave and an effective longitudinal mass, $m_{\|}$, for the inversion carriers in the 2-d energy subband, the mobility is calculated as,

$$\mu_L = (q\hbar^3\rho c_{l2}^2 d)/(m_{\|}^2 E^2 k_B T). \quad (2.25)$$

Considering only the 2-d ground state eigenvalue $E_x(0)$ for the triangular potential well, and given the transverse field as,

$$E_X = E_X(0)/qd = (4\pi/\varepsilon_s)(Q_{DEP} + Q_{INV}) \quad (2.26)$$

it is easily shown that d (the average distance of the inversion layer charge from the interface) has a $(N_{DEP} + N_{INV})^{-1/3}$ dependence and hence the mobility is proportional to $T^{-1}(N_{DEP} + N_{INV})^{-1/3}$.

The theory was later refined by Ezawa, Kawaji and Nakamura [29] who introduced the term 'surfon' to describe acoustic phonons that satisfy the interface boundary conditions, but have bulk and surface modes of vibration. Their analysis included various vibrations modes for the surfons and their electron interactions, as well as the effects of anisotropic conductivity tensors for different crystal orientations. Inter-subband transitions and intervalley scattering were not considered. Some of the

remaining discrepancy in the theory, on the order of 6X larger mobility than that measured, was attributed to optical phonon interactions and possible differences between the assumed bulk values of the constants, such as polarizability, ε, and their actual values near the $Si/SiO_2$ interface.

For temperatures below 100°K the measurements of Sah, Ning and Tschopp [25] showed that the mobility due to lattice scattering, $\mu_L$, varies as $7.4x10^5/T$ by using the approximation by Debye and Conwell for $\mu_I$ [30],

$$1/\mu_L = 1/\mu_{exp} - 1/\mu_I \tag{2.27}$$

where $\mu_{exp}$ and $\mu_I$ are the experimental and ionized impurity values of mobility. At higher temperatures (>150°K) Sah-Ning-Tschopp [25] reformulated the theory to account for optical or intervalley phonon scattering and found

$$\mu_L = 10^8/T^2. \tag{2.28}$$

This solution was obtained by replacing the deformation potential, the phonon energy, and the occupation number for acoustical phonons with their optical counterparts which was also employed by Luong and Shaw [31]. The two relaxation times for the optical and acoustical cases are assumed independent,

$$\tau^{-1} = \tau_A^{-1} + \tau_O^{-1}. \tag{2.29}$$

The resulting expression for mobility is given in terms of the purely acoustical dependence $\mu_A=7.4x10^5/T$, the optical and acoustical ratio of the deformation potential constants $Z_O/Z_A$, and the optical phonon energy, $\hbar\omega_q$. A good fit to their mobility data was obtained for T=20-300°K and a range of oxide and interface trap densities when,

$$Z_O/Z_A = 2.3 \tag{2.30}$$

$$\hbar\omega_q/k_B = 650\pm50^\circ\ K \tag{2.31}$$

## 2.6 Surface Roughness Scattering

The possibility of mobility reduction due to the atomic irregularity at the $Si/SiO_2$ interface was analyzed by Cheng and Sullivan [32-34]. Under very controlled processing conditions, they were able to fabricate transistors using a variety of oxidation conditions to alter the quality of the $Si/SiO_2$ interface and a range of interface trapped charge densities, $N_{IT}$. Measurements were performed at liquid helium temperature (4.2°K) to minimize the interference of phonon scattering. Mobility was extracted at high transverse fields or high inversion carrier densities to emphasize the effects of surface roughness by bringing the mobile carriers closer to the interface. The observed strong $N_{INV}^{a}$ ($-1 < a < -1.5$) dependence of the surface mobility at high fields was attributed by these authors to atomic surface inhomogeneity.

The analysis for modeling this scattering mechanism is similar to that of surface charges with a random spatial distribution in the oxide. In an ideal situation the $Si/SiO_2$ interface would be treated as a perfect plane. Differences in the crystal structure of the Si substrate and the amorphous nature $SiO_2$, are immediately evident in their energy bands as well as their electrical and thermal conductivity properties which prevent the $Si/SiO_2$ interface from being completely planar. To model the apparent atomic irregularity in the direction perpendicular to the interface, a random spatial displacement, $\Delta x(R)$, is imposed upon the potential $V(x)$ of an ideal planar surface. The perturbed Hamiltonian is given by,

$$H = -\hbar^2\nabla^2/2m^* + V[x - \Delta x(R)] \tag{2.32}$$

$$\delta V = V[x - \Delta x(R)] - V(x) = \Delta x \bullet (\partial V/\partial x) \tag{2.33}$$

and $\delta V$ is the first order perturbation of the potential. Assuming the same form for the ground state wave function, $\Psi$, as Stern and Howard [19], though translating the boundary condition of $\Psi(x=0)=0$, the matrix element for $\delta V$, $<\zeta(x)|\delta V|\zeta(x)>$ and the scattering rate, $\Gamma_{kk'}$, may be calculated. The derived relaxation time, $\tau(k)$, exhibits a strong dependence on the inversion carrier concentration and two adjustable parameters related to the Gaussian distribution assumed for $\Delta x(R)$,

$$1/\tau = (144\pi^2 q^4 L^2 \Delta^2 m_{\|}/\varepsilon_s^2 \hbar^3)[N_{DEP} + (11/32)N_{INV}]^2$$
$$*\int(1-\cos\Theta)\exp[-(1-\cos\Theta)k^2L^2/2] \qquad (2.34)$$

where $\Delta$ is the mean asperity of the perturbation to the ideal plane and L is the correlation length of the Gaussian distribution (Figure 6 in [32]). Assuming completely independent scattering mechanisms, the reciprocal relaxation times for surface roughness and the Coulombic scattering are added and used to find the mobility in the usual manner,

$$1/\tau = 1/\tau_{sr} + 1/\tau_{coul} \qquad (2.35)$$

$$\mu = (q/m)<\tau> \qquad (2.36)$$

Since various surface preparations have been used in the industry and reported in the literature, and since the thermal oxide growth conditions (dry, wet, with or without HCl, TCA, and nitrogen, varying temperature, etc.) also vary from one process to the next, large variations in the asperity and correlation would be expected. Hence it would not be unusual to find significant process variation in $\mu_{sr}$ and its dependence on $N_{INV}$. Matsumoto and Uemura [35] refined the work of Cheng et. al. [33] by including the effects of screening by the inversion layer and by selfconsistent calculation of V(x) using the variational approach and the Stern and Howard [19] ground state wave

function. They also defined an expression for the effective field in the semiconductor as,

$$E_{eff} = \int \zeta(x)\delta V \zeta^*(x)dx = 4\pi q^2/\varepsilon_s[(N_{INV}/2)+N_{DEP}] \quad (2.37)$$

where the first term (inversion charge) in the parentheses will dominate at high fields as expected. The relaxation time can therefore be expressed as a function of $E_{eff}^2$. Harstein, Ning, and Fowler [36] have also measured the effective mobility at very low temperatures while varying the oxide charge in their samples and have experimentally separated the effects of Coulombic and surface roughness scattering using the Mathiesiens rule. More recent measurements by Takagi [37] at 77°K have shown close agreement to the theoretically predicted $(N_{INV})^{-2}$ dependence for electron mobility due to surface roughness whereas the mobility for holes demonstrates a weaker $(N_{INV})^{-1}$ dependence. Agostinelli [38] speculates that this may be due to the difference in the distribution of holes in the inversion layer further away from the interface as suggested by Moglestue's [39] self-consistent calculations on <100> silicon.

## 2.7 Physical and Semi-empirical Models

It would appear that out of the three different scattering mechanisms affecting the inversion layer mobility, surface roughness scattering is the most difficult to accurately model without experimental parameter fitting because of surface processing dependences. Yet it should be noted that some of the recent experimental work has shown a universal behavior for surface roughness scattering in devices processed by

different groups [37, 40-42]. In providing a physically based mobility model, Sah [10, 14-16] summarized the various scattering mechanisms affecting mobility as follows:

Electrons

| | | |
|---|---|---|
| $\mu_{OnLA} = 7.4x10^5/T$ | Surface acoustical phonons | (2.38) |
| $\mu_{OnLO} = 1.0x10^8/T^{1.9}$ | Surface optical phonons | (2.39) |
| $\mu_{OnOX} = 10^3(3x10^{11}/N_{OX})(T/80)$ | Oxide charge | (2.40) |
| $\mu_{OnDP} = 10^2(N_{DP}L_{DP}^2)^{-1}(T/300)^{1.5}$ | Surface dipoles | (2.41) |
| $\mu_{OnSR} = 1.5x10^{29}q^2/(\|Q_B\|+\|Q_{INV}\|)^2$ | Surface roughness | (2.42) |
| $\mu_{OnCI} = 8.5x10^8/(N_{ION})^{1/3}$ | Ionized impurities | (2.43) |

where $Q_B$ is the bulk charge density and $N_{OX}$ is the oxide charge density. The total mobility, $\mu_o$, is found by Mathiessen's rule by adding the mobility terms listed above as $\mu^{-1}$. The hole mobilities were approximated by scaling the electron mobility by the hole/electron bulk mobility ratio ($\mu_p/\mu_n$=478/1423) [14-16]. The transverse and longitudinal field dependences are also given [10] as follows:

| | | |
|---|---|---|
| $\mu = \mu_o[1+(\|E_Y\|/E_{CL})^\gamma]^{-1/\gamma}$ | Longitudinal Fields | (2.43) |
| $\mu = \mu_o[1+(\|E_Z\|/E_{CT})]^\delta$ | Transverse Fields | (2.44) |
| $E_{CL} \simeq \Theta_{sat}/\mu_o = 1.02x10^7/\mu_o$ | Electrons | |
| $E_{CL} \simeq \Theta_{sat}/\mu_o = 0.75x10^7/\mu_o$ | Holes | |
| $E_{CT} \simeq 100$ kV/cm | | |

where $E_Y$ and $E_Z$ are the longitudinal and peak transverse fields in the silicon surface layer, $E_{CL}$ and $E_{CT}$ are the critical longitudinal and transverse fields and the constants, $\gamma$ and $\delta$, are empirical constants which vary slightly with temperature and both longitudinal and transverse electric fields.

Various other semi-empirical mobility models have been developed for electrons [43-49] and holes [38] but as the term semi-empirical suggests, these models require a priori knowledge of the device characteristics to establish the various fitting parameters in the model. The model developed by Schwarz and Russek [43] which showed excellent agreement with the experimental data of various groups [25, 40, 42, 50] was extended by Shin et al. [45, 46] using a novel modeling approach, to account for the low-field and high-field mobility drop-off. The model by Shin et al. model extracts the functional dependence of the inversion layer mobility on local transverse and longitudinal electric fields, substrate doping concentration, fixed interface charge and temperature from the experimentally measured effective mobility, $\mu_{eff}$. Their model, which was implemented in the PISCES 2-d device simulator, was shown to have good agreement with experimental $I_D$-$V_G$ and $I_D$-$V_D$ data. These models though do not account for the Coulombic scattering due to trapped oxide charge build-up during stress or the distribution of this charge which are the primary topics of this thesis.

The following chapter will the discuss the theory of operation and fabrication of the BiMOST test structure and various techniques used to extract the saturation and the conductivity effective mobilities.

# CHAPTER 3
# BiMOST FABRICATION AND OPERATION AND EFFECTIVE MOBILITY EXTRACTION

In chapter 2 the work of previous authors on the scattering mechanisms affecting the inversion carrier effective mobility was reviewed. This chapter consists of two sections on: 1) the fabrication and operation of the BiMOST test structure and 2) a detailed description of the mobility extraction procedures. The following chapter, chapter 4, will describe their applications to the experiments on the effects of charging and discharging oxide traps on the degradation of the mobility, drain saturation current, and threshold voltage.

## 3.1 BiMOST Fabrication and Operation

The BiMOST test structure, shown in Fig. 3.1, was employed in this study because of the versatility it provides for studying the gate oxide layer. The physical aspects which make this structure unique are that it combines a vertical n/p/n or p/n/p bipolar junction transistor (BJT) with an n- or p-channel MOST on the surface. This allows one to stress the $SiO_2$/Si interfacial layer, inject charges into the gate oxide and characterize the resultant degradation by methods not available using the MOS or

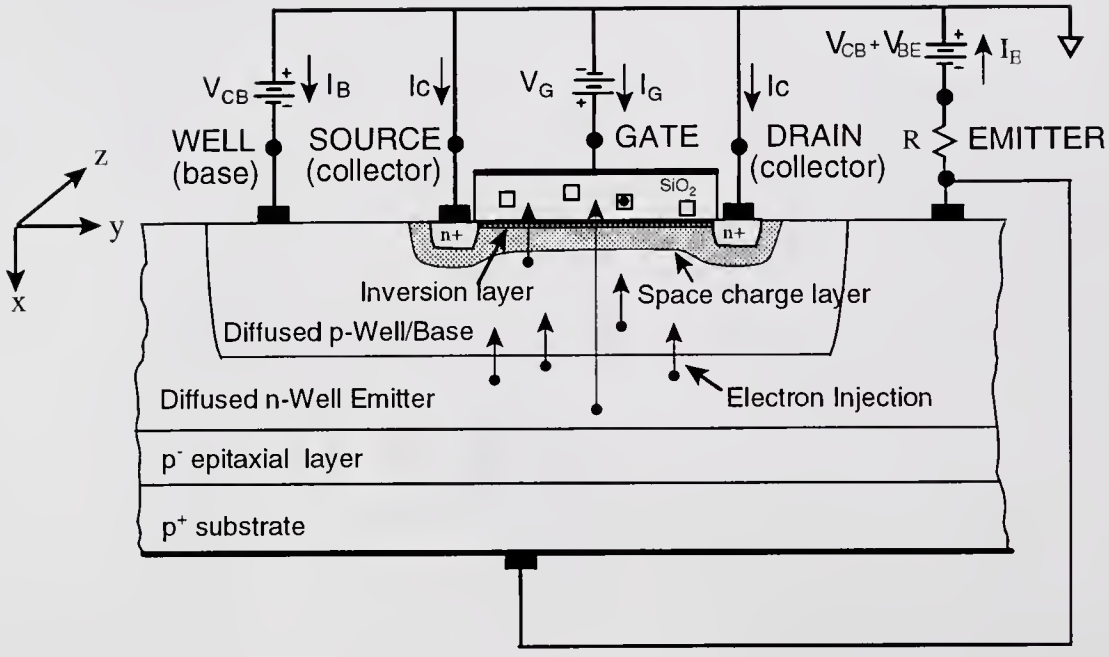



Figure 3.1 N-channel BiMOST test structure biased for substrate hot electron injection (SHEi).

bipolar transistors or the MOS capacitor alone. These features will be discussed in the following section.

The BiMOST structure is in fact present in all CMOS and BiCMOS technology today. A typical CMOS wafer and chip fabrication process begins with a highly doped p-type silicon wafer of 6-inch or 8-inch diameter and 500-micron thick (to be denoted by p+Si where + signifies high dopant impurity concentration which is the boron acceptor for p-type Si). On the atomically flat and polished wafer surface is epitaxially grown a thin lowly doped p-type silicon layer (to be denoted by p–Si layer where the – or minus sign signifies low dopant impurity concentration). Using thermally grown or deposited silicon dioxide ($SiO_2$), silicon nitride ($Si_3N_4$), and polycrystalline silicon films as a penetration mask and photolithography for pattern definition, the epitaxial surface is selectively implanted with n-type (phosphorus or arsenic) and p-type (boron) impurities to form the n-well and p-well in which the p-channel and n-channel MOST's, respectively, are then built respectively. To achieve a good interfacial layer for oxide growth, improve the surface mobility and minimize short channel effects, the impurity profile in the wells is highly retrograded in today's production MOSTs with <0.5micron channel length and in future state-of-the-art 0.1μm channel length MOSTs [7]. A typical retrograde profile will have a peak impurity concentration on the order of ~$10^{18}cm^{-3}$ at about 500Å from the $Si/SiO_2$ interface in the ion implanted silicon well while the impurity concentration at the $Si/SiO_2$ interface is 1-2 orders of magnitude below this peak. If the inversion layer of the MOST surface channel is about 30-100Å thick, as discussed in chapter 2, then the highly retrograde profile of ionized impurity centers in the well will play an important role in determining the effective mobility.

Summarized briefly, the following steps in the CMOS (fabrication) process would first thermally grow the very thin (3.5nm for next generation and 6nm for Pentium P-6 announced by Intel in December 1994) gate oxide on the epitaxial surface and then deposit a polysilicon layer (poly-Si or just poly) over the entire surface. Next, using the poly as the ion implantation mask by etching holes or patterns through the poly and the gate oxide layers using photolithography (known as the self-aligned process) shallow n-type and p-type impurity ion implantation through the holes is made to give the n+ and p+ source and drain islands and to dope the polysilicon gate to high n+ or p+ conductivity. On a p+Si or n+Si 6" or 8" wafer, both a p-channel BiMOST with a vertical p/n/p BJT and an n-channel BiMOST with a vertical n/p/n BJT can be fabricated. A cross-sectional view of the nBiMOST is shown in Fig.3.1 which is fabricated on a n+Si wafer.

Some of the MOSTs and BiMOSTs measured in this thesis investigation were obtained from industrial mentors. They were completely processed in their state of the art production facilities, hence, represent the cleanest condition attainable. Large area pBiMOSTs and nBiMOSTs were also fabricated by this candidate in our university clean room fabrication laboratory, at high yields, and by other graduate students and professors in our research group. These large area transistors were fabricated on 1"x1" wafers which were cut from 6" or 8" diameter wafers provided by industrial mentors who first oxidized the n/p-epitaxy/p+substrate and p/n-epitaxy/n+substrate 6"-8" wafers. All the remaining fabrication steps, except ion implant, were carried out by this candidate in our own clean-room device fabrication laboratory, which included self-aligned process to define the gate, implant the source, drain, and poly-gate regions

(by a California silicon chip foundry), and evaporate aluminum contacts on the front and back of the wafers. The industrial mentor supplied MOSTs were rectangular with L=W=100μm to L and W less than 0.5μm. Those fabricated by this candidate were large concentric circles with L=150μm and a large gate area ($3.89X10^{-3}cm^2$). Gate oxide thickness covered the range of 3.5nm to 30nm.

One of the key advantages of the BiMOST test structure is that the oxide electric field, $E_{OX}$, the reverse bias voltage, $V_{CB}$, across the inversion layer or the collector/base junction and the injection current through the gate, $I_G$, can all be varied independently. This allows one to stress the oxide using the substrate hot electron injection (SHEi) technique at gate bias voltages as low as $V_G=V_{GT}$ near the threshold and well below the Fowler Nordheim tunneling voltage or tunneling electric field . For SHEi the vertical n/p/n bipolar transistor is operated in the forward active mode of the bottom emitter configuration with the bottom emitter-base junction ($V_{EB}$) forward biased and the n-channel/p-well space charge layer reverse biased. The forward emitter-base bias ($V_{EB}$) injects the minority carriers (electrons) from n-emitter into the p-base of the vertical n/p/n BJT. These minority carriers (electrons) diffuse through the p-base and, upon entering the surface space charge layer beneath the n-inversion channel, are accelerated towards the $Si/SiO_2$ interface by the electric field in the surface space-charge layer of the reversed biased collector/base and channel/base junction. If the accelerated electrons have enough kinetic energy at the interface to surmount the $Si/SiO_2$ electron energy barrier (3.13eV for electrons and 4.25eV for holes), they will be injected into the oxide conduction band (or valence band for holes injected in the pBiMOST). In the oxide layer the injected electrons, now labeled oxide electrons or electrons in the oxide

conduction band, are accelerated further by the oxide electric field, $E_{OX}$, as they transit toward the poly-Si gate electrode and exit the gate terminal to give the measured gate current. Only a small fraction of the injected oxide electrons will be trapped or expended via one of numerous trap charging-discharging, generation, neutralization, and even annihilation mechanisms in the oxide or at the poly-gate/$SiO_2$ and $SiO_2$/Si interfaces. During the stress or SHEi, the gate current is maintained at a constant value by varying the d.c. forward bias on the emitter/base junction. In former reports, verified in this thesis, SHEi is areally uniform, across the length of the channel, in contrast to the ac avalanche injection or the dc channel hot carrier (CHC) or channel hot electron (CHE) stress techniques. Areal uniformity greatly simplifies the analysis of the MOST IV and CV characteristics since any distortion of the IV and CV curves due to nonuniform charge in the oxide can be misinterpreted as interface traps generated during the stress. By maintaining the reverse bias voltage on the collector/base junction below breakdown, SHE injection remains uniform and enables us to evaluate the initial quality (or oxide and interface trap densities) of the oxide and Si/$SiO_2$ interface, and also the effects of post oxidation processing undertaken by us.

## 3.2 Measurement of $\mu_{lin}$

The effective mobilities (linear and transconductance) of electrons and holes has been measured extensively in the literature using the MOST. Leistiko, Grove and Sah [51] measured the dc or differential conductance, $g_d$, of the inversion layer at low drain voltages or in the linear $I_D$-$V_D$ range, which was defined as

$$g_d = (W/L)q\int\sigma(x)dx \tag{3.1}$$

where $\sigma(x)$ is the conductivity of the inversion layer at a depth x below the interface defined by $\sigma(x)=q\mu(x)N(x)$ where $\mu(x)$ and $N(x)$ are the electron mobility and electron concentration at a distance x from the $SiO_2/Si$ interface (x=0). Thus, $\sigma(x)$ is the electron conductivity (siemen or mho/cm) at a depth x in the inversion channel. The length and width of the channel are L and W. The integration covers the inversion layer thickness (x=0 to $x_i$). The drain conductance, effective conductivity or linear mobility, and inversion charge density ($q/cm^2$) are then,

$$g_d = (W/L)q\int\mu(x)N(x)dx = (W/L)\mu_{lin}Q_{INV} \tag{3.2}$$

$$\mu_{lin} = g_d/[(W/L)Q_{INV}] = \int\mu(x)N(x)dx \,/\, N_{INV} \tag{3.3}$$

$$N_{INV} = \int N(x)dx \equiv Q_{INV}/q. \tag{3.4}$$

Approximating L and W of the large area devices by their drawn length and width, one needs only to measure the drain conductance, $g_d$, and inversion charge, $Q_{INV}$, to extract $\mu_{lin}$.

In this investigation, the drain conductance is calculated from the experimental dc $I_D$-$V_{DS}$ characteristics in the linear region ($V_{DS} = V_D - V_S < 100mV$) at very small longitudinal electric fields in the channel. The channel inversion charge density can either be measured using the approximation

$$Q_{INV} = C_{ox}(V_G - V_{GT}) \tag{3.5}$$

or by two ac capacitance techniques to be described. Although the value of $C_{ox}$ in (3.5) can be accurately determined using large area capacitors, the threshold voltage, $V_{GT}$, is rather ill-defined in weak inversion near $V_{GT}$, making (3.5) very inaccurate.

A more accurate method for extracting $Q_{INV}$, known as the 'Split-CV' method, was introduced by Koomen [11]. He used it only to study interface states in the inversion range. In this method the gate capacitance contributions of the source/drain/inversion layer ($C_d$+$C_s$) are separated ('split') from those of the bulk, $C_b$, shown the in Figure 3.2 and they can be easily measured using the standard 3-terminal capacitance meter. The assumptions are that the small signal excess majority carrier charge is supplied by the bulk current $dI_B$, whereas the contributions from interface state, $\Delta n_{IT}$, and excess minority carrier inversion charge, $\Delta n$, are supplied by $dI_D$ and $dI_S$. Thus,

$$C_d + C_s = (1/\omega)(dI_D + dI_S)/dV_G \tag{3.6}$$

$$C_b = (1/\omega)dI_B/dV_G \tag{3.7}$$

If the interface charge density is low, then $C_d$+$C_s$ maybe integrated over $V_G$ to give $Q_{INV}$ from weak to strong inversion,

$$\int(C_d + C_s)\, dV_G = qN_{INV} = Q_{INV} \tag{3.8}$$

This Koomen method was first implemented by Sodini, Ekstedt and Moll [52] to measure the effective conductivity or linear mobility, $\mu_{lin}$.

The exact method for measuring the conductivity mobility in a surface inversion channel was suggested and demonstrated by Shiue and Sah [53]. They employed the frequency dependencies of the ac conductance and capacitance of the channel treated as a distributed one-dimensional transmission line. They demonstrated consistency in the linear or effective conductivity mobilities calculated from the experimental input admittance data of the MOS channel transmission line in the subthreshold and inversion ranges. This exact method involved measuring the input admittance

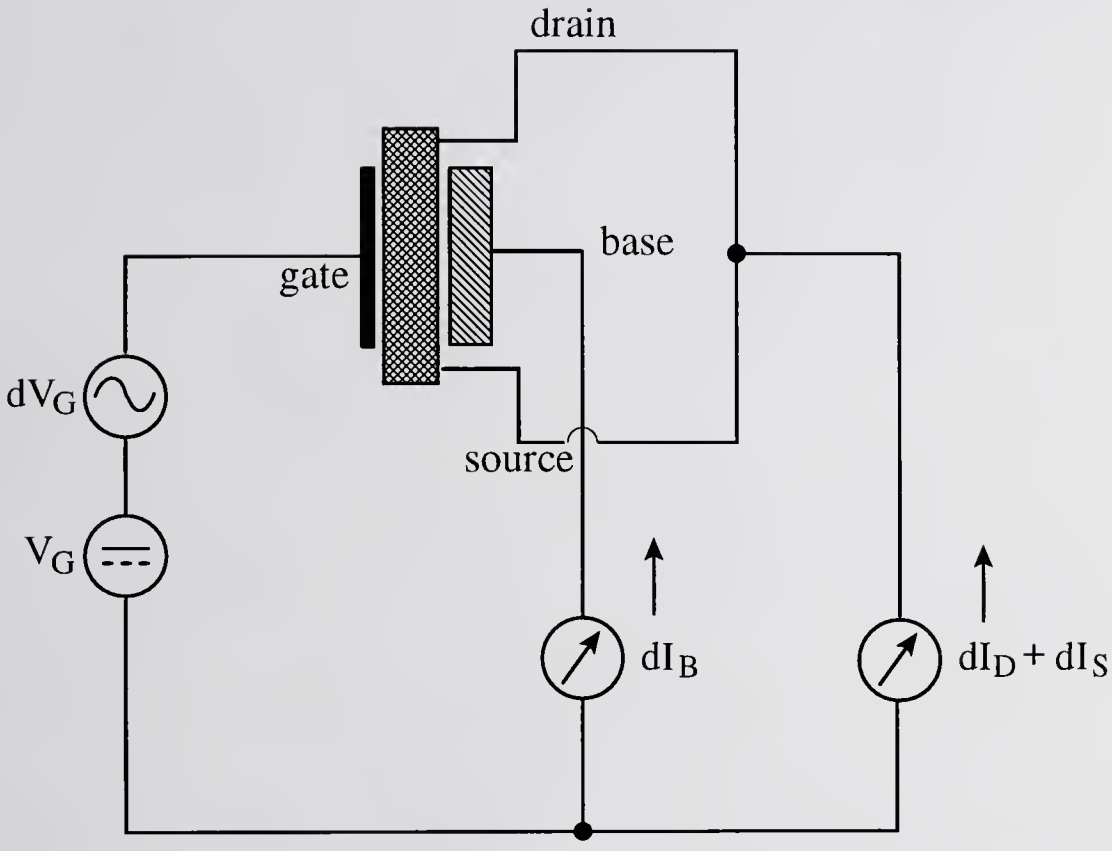



Figure 3.2 Split - CV or low frequency $C_{inv}$-$V_G$ measurement setup [33].

(capacitance and conductance) of the surface channel and analyzing the data using a distributed-transmission line model known as the circuit technique for semiconductor analysis (CTSA) [54, pp.160-164]. The CTSA equivalent circuit for an MOST, Fig. 3.3a [54, p.164], is synthesized using a small-signal expansion of the Shockley equations. The $C_{dg\text{-}overlap}$ and $C_{sg\text{-}overlap}$ are the drain and source overlap capacitances. $C_{dep}(y)$ is the distributed capacitance of the depleted layer of the surface space-charge layer. The charge storage capacitance of the electrons in the inversion channel, $C_n(y)$, is related to the electron concentration (number per unit volume), N(x), by

$$C_n = \int (q^2/k_B T) N(x) dx = (q^2/k_B T) N_{INV} \quad (F/cm^2) \tag{3.9}$$

where

$$N_{INV} = \int N(x) dx \quad (\#/cm^2) \tag{3.10}$$

Similarly, the conductance element of the channel is defined by

$$G_n = \int q\mu(x) N(x) dx \quad \text{(Siemen or mho)} \tag{3.11}$$

$$\equiv \mu_{lin} \bullet q N_{INV}$$

$$\mu_{lin} \equiv \int \mu(x) N(x) dx \,/\, N_{INV} \tag{3.12}$$

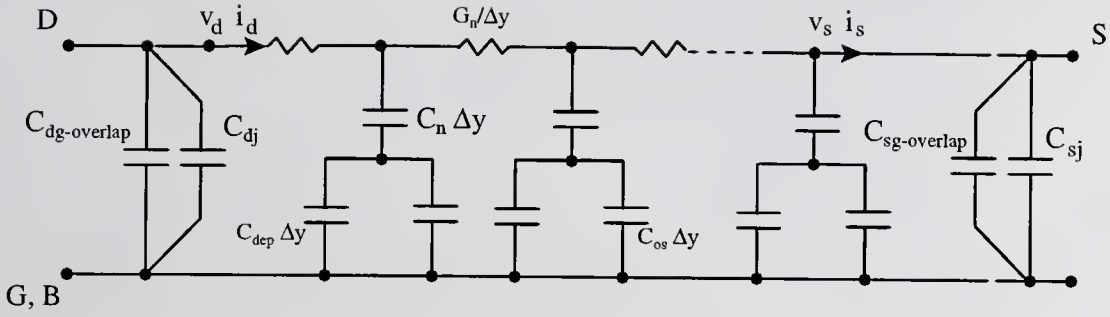
which provides the rigorous proof of the definition given by (3.3).

To find $C_n$ and hence $N_{INV}$, the CTSA circuit was simplified by ac short-circuiting the gate, source and substrate (Fig. 3.3b). The distributed capacitance element C(y) and the transmission line equations relating the small-signal input ($v_d$, $i_d$) to the output ($v_s$, $i_s$) are,

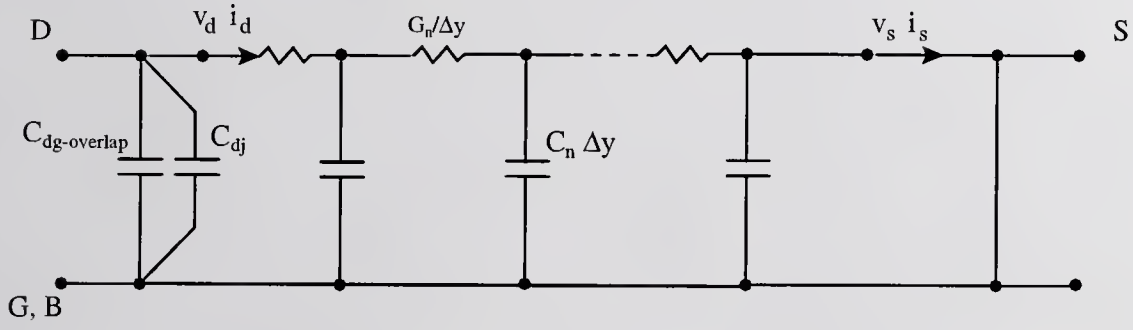
$$C = C_n(C_{dep}+C_{ox})/[C_n+(C_{dep}+C_{ox})], \tag{3.13}$$

$$v_d = v_s \cosh(\gamma L) + Z_o i_s \sinh(\gamma L), \tag{3.14}$$

$$i_d = (v_s/Z_o)\sinh(\gamma L) + i_s \cosh(\gamma L), \tag{3.15}$$




(a)




(b)

Figure 3.3a and 3.3b Distributed Transmission Line or CTSA model [32].
(a) Gate and Substrate ac short - circuited and
(b) Gate, Source and Substrate ac short - circuited

$$Z_o = [1/j\omega CZG_nZ]^{1/2} = (q^3/k_BTW)N_{INV}^2\mu_{lin}, \quad (3.16)$$

$$\gamma = [j\omega C/G_n]^{1/2} = [j\omega(q/k_BT)/\mu_{lin}]^{1/2} = (j\omega/D_{lin})^{1/2} \quad (3.17)$$

where W is the channel width, L is the channel length, $Z_o$ is the characteristic impedance, $\gamma$ is the propagation constant, $D_{lin}=(k_BT/q)\mu_{lin}$ is the linear or effective diffusivity, and $\omega$ is the measurement frequency. The measured short circuit capacitance, $C_{sc}$, approaches a value of CLW/3 when the measurement frequency is much smaller than the characteristic frequency given by,

$$f_o = (GW/L)/3\pi(CLW/3) = (1/\pi L^2)(G_n/C) \rightarrow D_{lin}/(\pi L^2). \quad (3.18)$$

where the asymptotic expression is for weak inversion when $C_n << C_{dep} + C_{ox}$. If the depletion and oxide capacitances, $C_{dep}$ and $C_{ox}$, can be obtained from the CV curve of a large area capacitor, then, the value of $C_n$ and $N_{INV}$ can be determined.

It is noted that by dc grounding the bulk of the transmission line and ac short-circuiting the source and drain, the input capacitance between the gate and source/drain is identical to $C_d+C_s$ in Koomen's analysis. This provides a rigorous theoretical proof for Koomen's empirical assumptions.

A typical split-CV or $C_{inv}$-$V_G$ measurement, between gate and the source/drain (base and emitter are dc grounded) of an n-channel BiMOST device, is given in Figure 3.4. The integrated Equation (3.8) gives the inversion charge density versus the gate bias $V_G$ which is also shown in Figure 3.4. Figures 3.5 and 3.6 illustrate the corresponding prestress linear and saturation current-voltage characteristics of the n-channel BiMOST. The drain current saturation condition is given by $V_D = V_G > V_{D\text{-}sat} = V_G - V_{GT}$. By extracting the drain conductance from the linear $I_D$-$V_{GS}$ for three

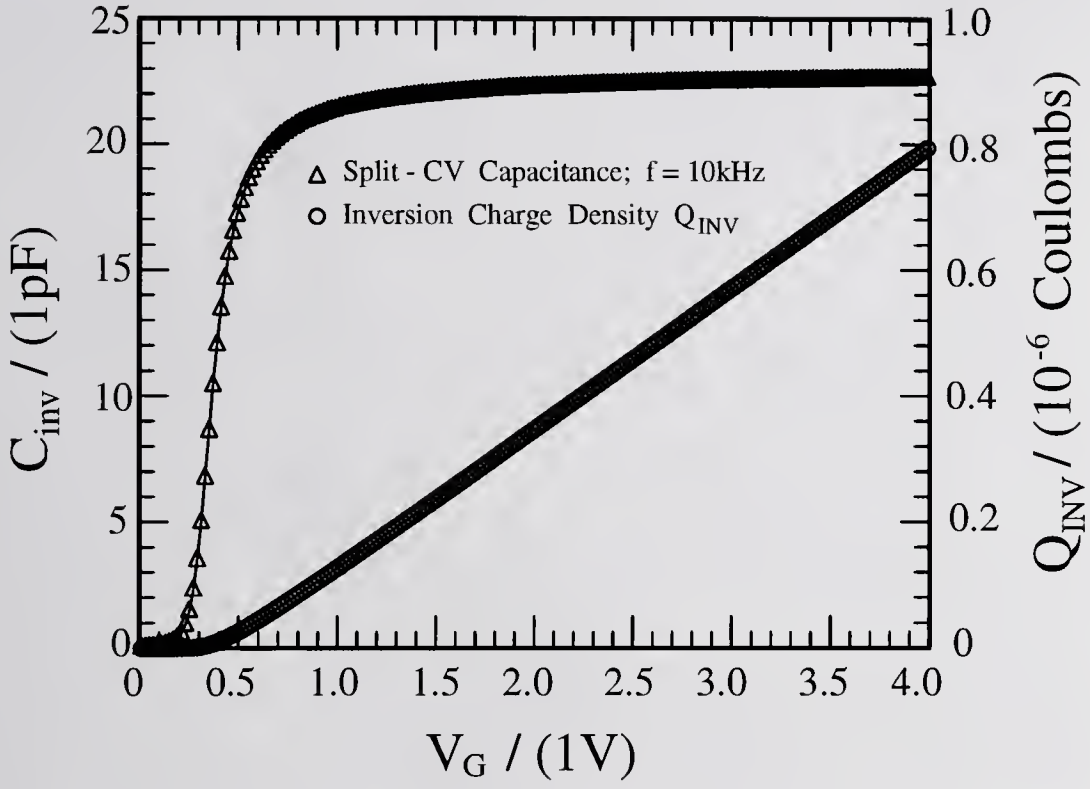



Figure 3.4 Initial prestress Split-CV measurement @10kHz for an n-channel BiMOST with gate area = 1.0E-4 $cm^2$ and an oxide thickness Xox = 150 A Temperature = 295K.

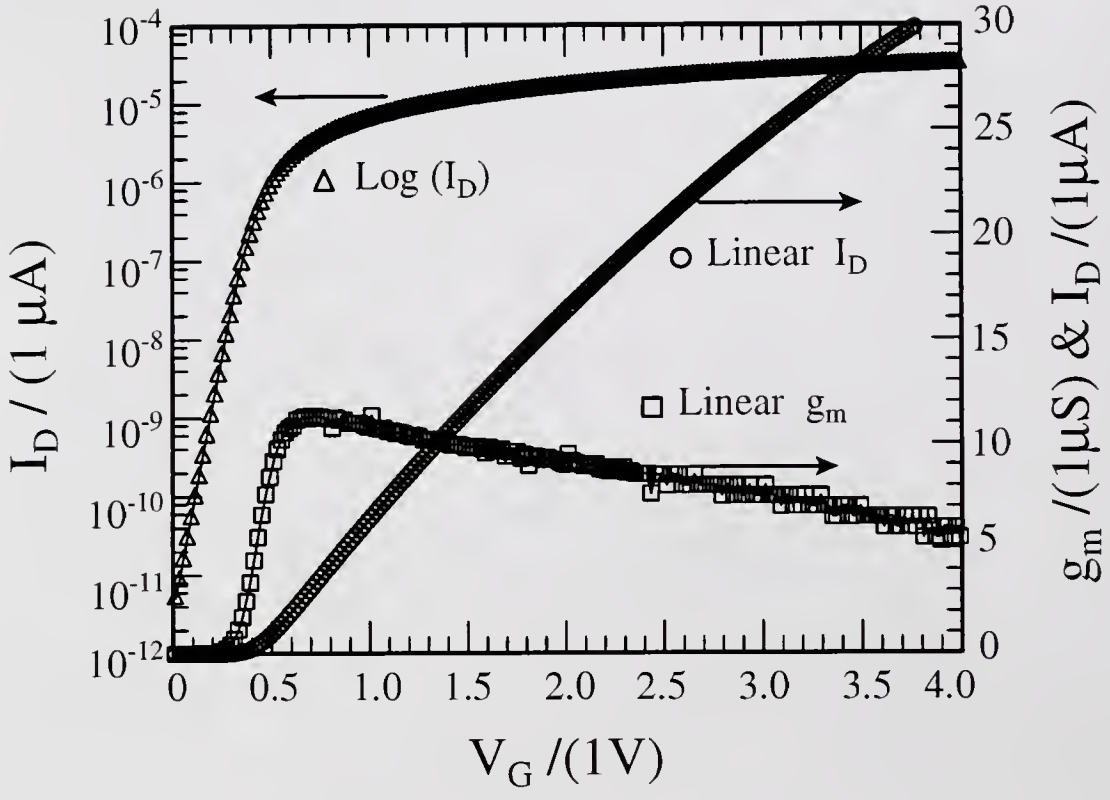



Figure 3.5 Linear and logarithmic plot of the $I_D$-$V_G$ and $g_m$-$V_G$ characteristics for an n-channel BiMOST with gate area = 1.0E-4 $cm^2$ and an oxide thickness $X_{OX}$ = 150A at Temperature = 295K.

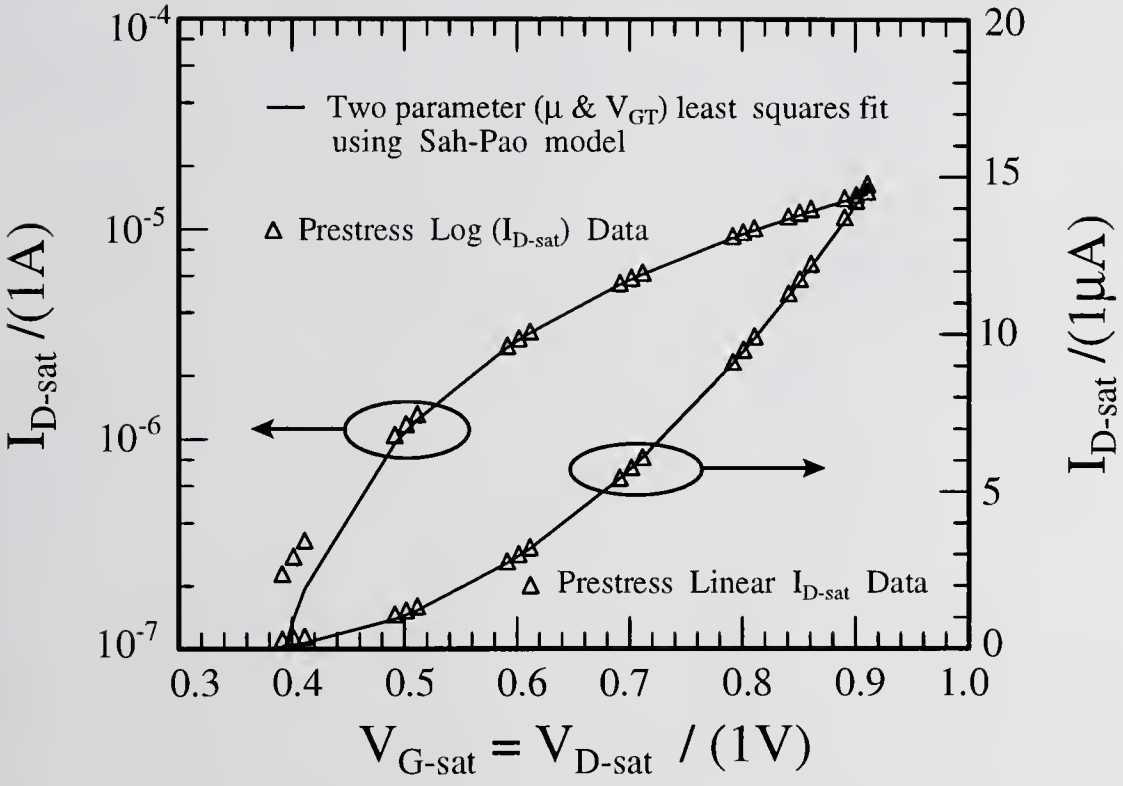



Figure 3.6 Prestress satureation $I_{D-sat}$ versus $V_{D-sat} = V_{G-sat}$ data (triangle marker) and a corresponding 2-parameter fit to the mobility and the threshold voltage using the Sah-Pao [35] model to include bulk charge effects.

values of $V_{DS}$ (90, 100, 110mV) the prestress effective conductivity or linear mobility (Fig. 3.7) can be calculated using equation 3.2.

The second effective mobility investigated in this thesis was the mobility in the drain-current saturation range, $\mu_{sat}$. It was extracted from the experimental $I_{D\text{-}sat}$ vs $V_{G\text{-}sat}$ data by least-squares-fit (LSF) the data to the Sah-Pao MOST d.c. equation with bulk charge [55]. The two LSF parameters were $\mu_{sat}$ and $V_{GT}$ and the Sah-Pao equations are:

$$I_{D\text{-}sat} = (\mu_{sat}C_o(W/L)\{(V_{DS}^2/2) + V_B V_{DS}[1+(V_{DS}/2\phi_F)]^{1/2} - (4\phi_F V_B/3)[(1+V_{DS}/2\phi_F)^{2/3} - 1]\} \quad (3.19)$$

$$V_{DS} = V_{G\text{-}sat} - V_{GT} + V_B + (V_B^2/4\phi_F) - V_B[1+(V_B^2/16\phi_F^2)+(V_G - V_{GT} + V_B)/2\phi_F]^{1/2} \quad (3.20)$$

$$V_B = [4qN_A\varepsilon_s\varepsilon_o\phi_F]^{1/2}/C_{ox} \quad (3.21)$$

$$\phi_F = k_B T \log_e(N_{AA}/n_i) \quad (3.22)$$

where $N_{AA}$ is the acceptor concentration in the silicon and $n_i$ is the intrinsic carrier concentration. The temperature dependence of $n_i$ is given by [54, p.52]

$$n_i = 2.50939\times10^{19}(m^*/m)^{3/2}(T/300)^{3/2}\exp[-E_G/(2k_B T)] \quad (3.23)$$

where the energy gap, $E_G$, and the effective mass ratio, m*/m, are given by

$$E_G = 1.1700 + (1.059X10^{-5})T - (6.05X10^{-7})T^2 \quad (T<150^\circ K) \quad (3.24)$$

$$E_G = 1.1786 - (9.025X10^{-5})T - (3.05X10^{-7})T^2 \quad (T>150^\circ K) \quad (3.25)$$

$$m^*/m = (m_N m_P/m^2)^{1/2} = 0.81577+3.4353X10^{-3}T[1-(T/437.6)+(T/814.2)^2+(T/1356)^3. \quad (3.26)$$

$$m_N/m_P = 1.065/0.647 \neq f(T) \quad (3.27)$$

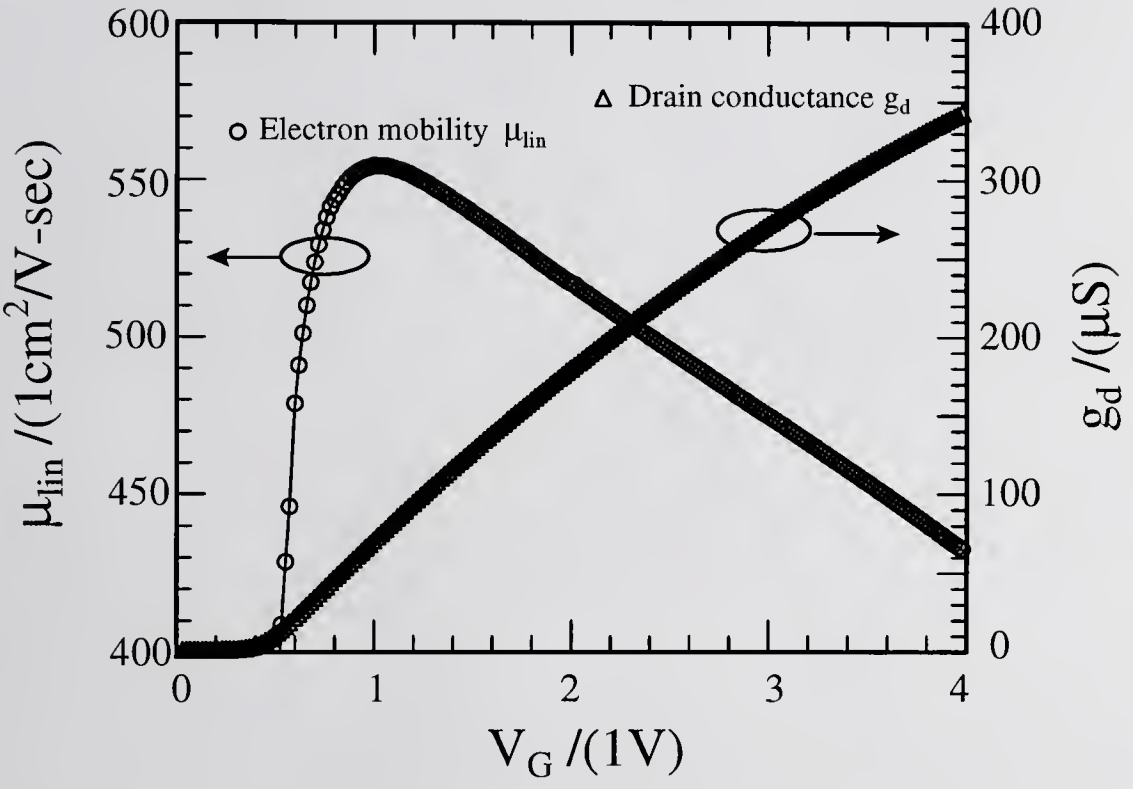



Figure 3.7 Drain (or channel) conductance, $g_d$, and conductivity effective electron or linear mobility, $\mu_{lin}$, as a function of the d.c. gate bias voltage, $V_G$.

Deionization of the dopant impurities at low temperatures is also taken into account by solving the following quadratic for the majority carrier hole concentration, P of an n-channel BiMOST,

$$P^2 + PK_A - KN_{AA} = 0 \tag{3.28}$$

$$K_D = (1/g_A)N_V \exp[-E_A/k_B T] \tag{3.29}$$

$$N_V = 2.50X10^{19} (m_p/m)^{1.5}(T/300)^{1.5} \tag{3.30}$$

where $N_V$ is the effective density of states in the valence band, and $m_p$ is the density of states effective mass in the valence band. The degeneracy factor, $g_A$, is assumed equal to 4 and the activation energy for boron is taken to be 45meV. Similar expressions are used for phosphorus in the p-channel case with $E_A$ replaced by $E_D$=44meV.

The shift in the gate threshold voltage, $\Delta V_{GT}$, as extracted from the aforementioned two-parameter fit to the drain-saturation-current data will be plotted unless otherwise noted since $V_{GT}$ can also be extracted from the linear $I_D$-$V_D$ characteristics.

As indicated above, $\mu_{lin}$ was obtained at $V_{DS} \rightarrow 0$ and $E_Y \rightarrow 0$ so there was no hot electron effect or mobility reduction with increasing longitudinal electric field. However, $\mu_{sat}$ was obtained at $V_D = V_G$ = power supply voltage, hence hot electron effects may be important in very short channels. This was not included in the Pao-Sah equation (3.19), but can be readily modified [10, pp.667-670] for short channels.

# CHAPTER 4
# OXIDE TRAP CHARGING AND DISCHARGING EXPERIMENTS

Chapter 3 reviewed the fabrication and operation of the very versatile BiMOST test structure and mobility extraction methods for the two effective mobilities, $\mu_{lin}$ and $\mu_{sat}$. In this chapter the effects of charging and discharging traps in the gate oxide layer on the two effective mobilities, the drain saturation current, and the threshold voltage will be demonstrated by experiments. The injection mechanism and the nature of the traps being charged and discharged during the stress cycles will also be discussed. The results in this chapter are obtained on the n-channel BiMOST and are therefore related to electron conduction in the surface channel. The results support the theory of increased Coulombic scattering as the net trapped oxide charge density increases, and decreased scattering as the net trapped oxide charge density decreases. Furthermore, the changes in $\mu_{lin}$, $\mu_{sat}$, $I_{D\text{-}sat}$, and $V_{GT}$ are shown to be consistent with the expected sign of the charging and discharging mechanism. The linear proportionality of the mobility change with positive and negative oxide charge density suggests a single species of oxide trap with three charge states (+, 0, –) as anticipated from the bridging oxygen vacancy or E' center.

Since the $I_{D\text{-}sat}$ measurement is taken at the condition of $V_D = V_G > V_G - V_{GT}$, the MOST may actually suffer CHEi stress during the poststress characterization. To limit any such measurement stress, the measurement voltages were kept low and only a

small number of triplet data points, with a minimum number of samples for noise-suppressing averaging, were measured at each of the predetermined voltages shown in Figure 3.6. To insure that the device is not inadvertently stressed during measurements, the linear- and saturation-IV and the split-CV were measured repetitively at the intended measurement voltages on an unstressed MOST to detect any shift in $V_{GT}$ during future poststress measurements. The results are shown in Figure 4.1 where the shift in the gate voltage was measured at a constant drain current of 1μA and plotted versus the measurement cycle to a total of 72 cycles. In the first 22 cycles only the linear IV and split-CV were measured while the remaining 50 cycles included the saturation IV measurement. Figure 4.1 shows that $\Delta V_{GT}$ is less than 0.2mV or the oxide charge changes by less than $3x10^8$ q/cm$^2$ (from $\Delta Q_{OT} = - C_o \Delta V_{GT}$ where $C_o = \varepsilon_o / X_{ox}$ is the oxide capacitance) after 72 cycles at an experimental resolution better than ±50μV (±$10^8$ q/cm$^2$). Thus, this test assures accuracy of the degradation data since the test shows that the MOST was not stressed significantly during the measurement part of the stress-and-measure (SAM) experiments on nBiMOSTs and nMOSTs undertaken in this thesis and described in the following sections and the next chapter.

## 4.1 Net Negative Charge Build-Up Due to SHEi

The first stress-and-measure or SAM experiment was to stress the BiMOST by SHEi at a constant 5MV/cm gate oxide electric field. The gate current was kept constant during the stress at $I_G$=3nA and the reverse bias on the collector base junction

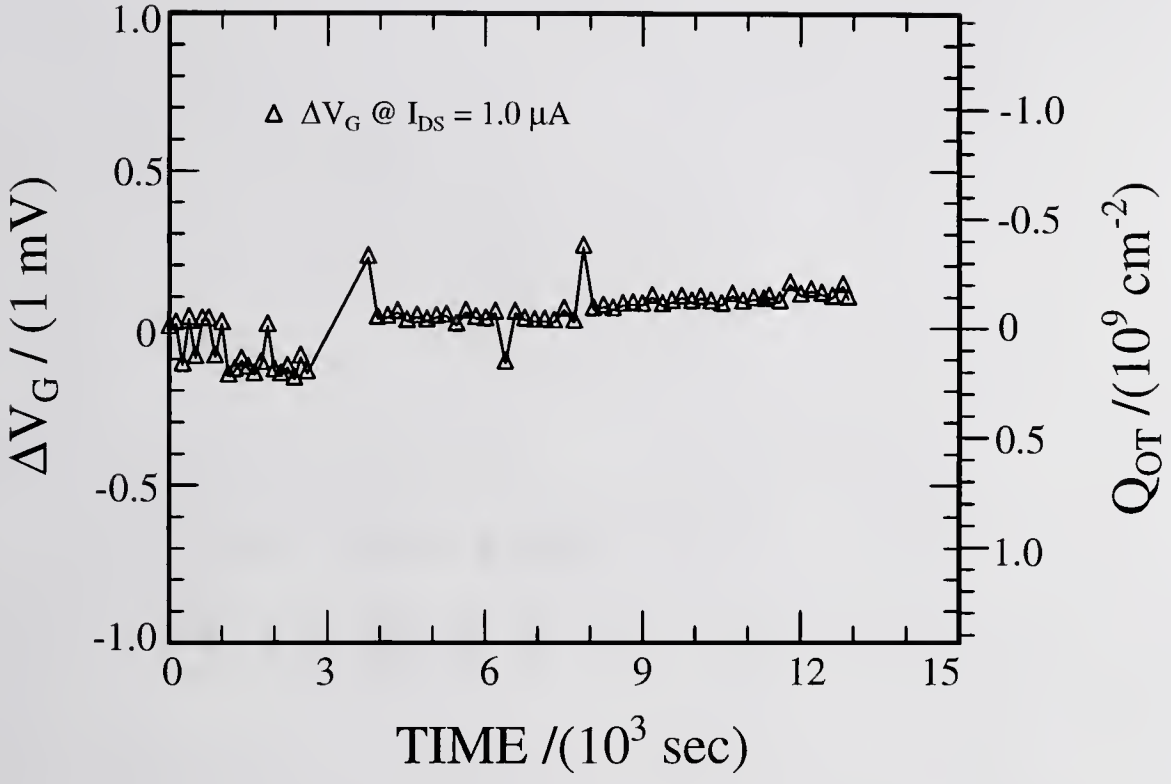



Figure 4.1 Ths shift in the gate voltage, $\Delta V_G$, of an n-channel BiMOST due to repetetive measurement of $I_D$-$V_G$, Split - CV, and saturation. $I_{D\text{-}sat}$ - $V_{G\text{-}sat}$ (=$V_{D\text{-}sat}$).

was kept constant at 4V ($V_{CB\text{-}breakdown} > 15V$). The shift of the following MOST characteristics and material parameters due to the SHEi stress were measured: linear and saturation $I_D$-$V_G$, transconductance $g_m$, split-CV, $Q_{INV}$, $\mu_{lin}$ and $\mu_{sat}$, and $g_d$. They are plotted as a function of $V_G$ in Figures 4.2a-d at two stress fluences, $N_{INJ} = 0$, 1.3 and $2.7\times10^{18}cm^{-2}$. The injection stress fluence is defined as the integrated electron current flowing through the gate oxide,

$$N_{INJ} = (1/qA)\int I_G \, dt \quad (electron/cm^2\text{-}sec) \tag{4.1}$$

where A is the gate area and $I_G$ is the d.c. gate current. In Figure 4.3a the effective conductivity or linear mobility is replotted as a function of the inversion charge density $Q_{INV}$, which is proportional to the effective field in the silicon surface, as derived in chapter 2, thus, this figure illustrates the true mobility degradation by eliminating the effect of $\Delta V_{GT}$. For comparison, the approximate linear mobility is also computed from the approximated inversion charge density using (3.5), $Q_{INV} \simeq C_{ox}(V_G - V_{GT})$. The approximate $\mu_{lin}$ versus the approximate $Q_{INV}$ is plotted in Figure 4.3b. The value of $V_{GT}$ used here was extracted from the linear $I_D$-$V_G$ near the peak $g_m$ which is the industry standard criteria. Comparing Figures 4.3a and 4.3b, it is evident that the approximate $Q_{INV}$ underestimates $\mu_{lin}$ due to overestimating $Q_{INV}$ from using (3.5), nevertheless, the decreasing trend in the mobility with increasing stress fluence, $N_{INJ}$, is still clearly evident in Figure 4.3b. These results are representative of the $X_{ox}$=170Å BiMOST with a gate area of A=100x100$\mu m^2$. The positive gate voltage shift indicates a buildup of net negative charge trapped in the oxide. The extracted threshold voltage shift, $\Delta V_{GT}$, is shown in Figure 4.4 versus the electron injection fluence through the gate. The repeatability of these results is monitored versus fluence rather than stress

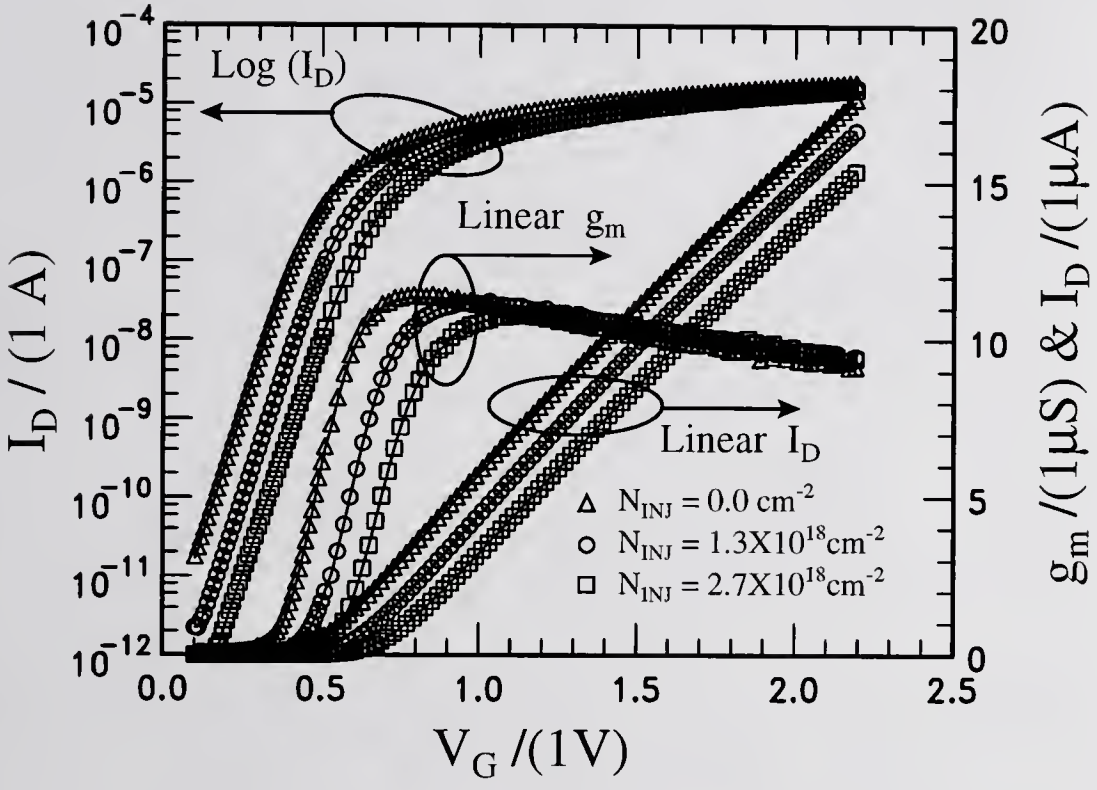



Figure 4.2 a Shift in the linear IV of an n-channel BiMOST due to SHEi stress at a constant $E_{OX}$ = 4MV/cm. The curves for three different fluences are plotted.

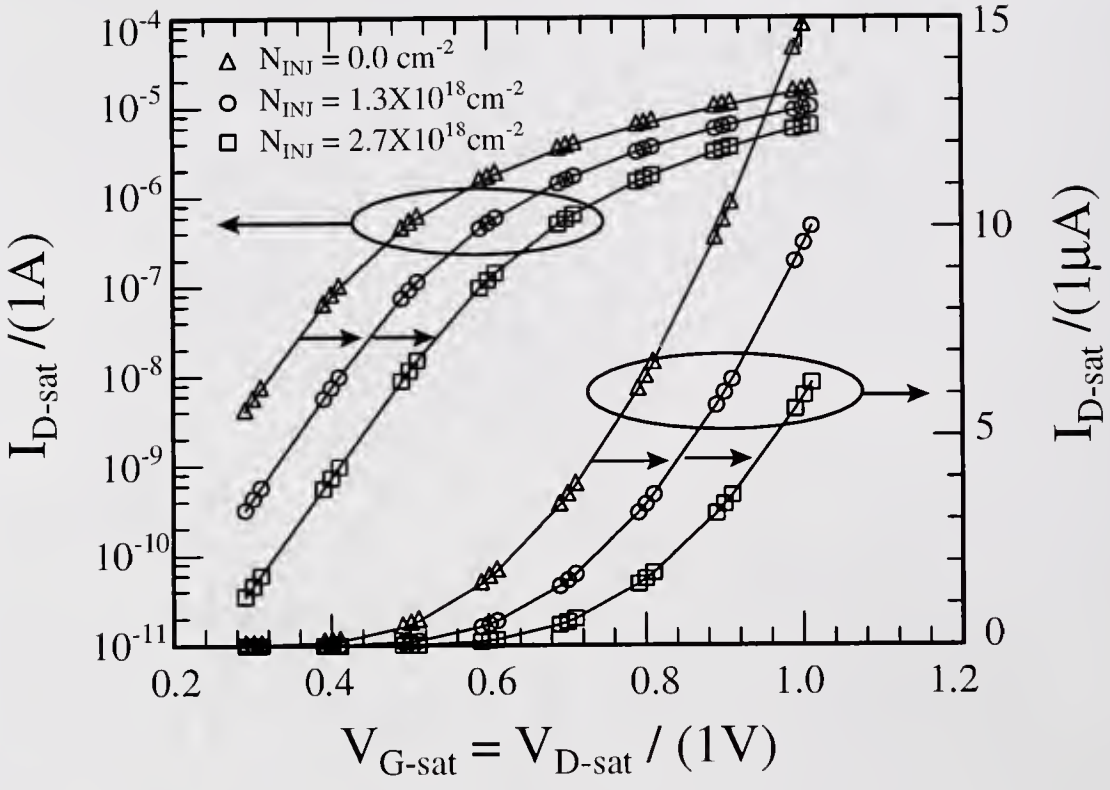



Figure 4.2 b Shift in the saturation IV of an n-channel BiMOST due to SHEi stress at a constant $E_{OX}$ = 4MV/cm. The curves for three different fluences are plotted.

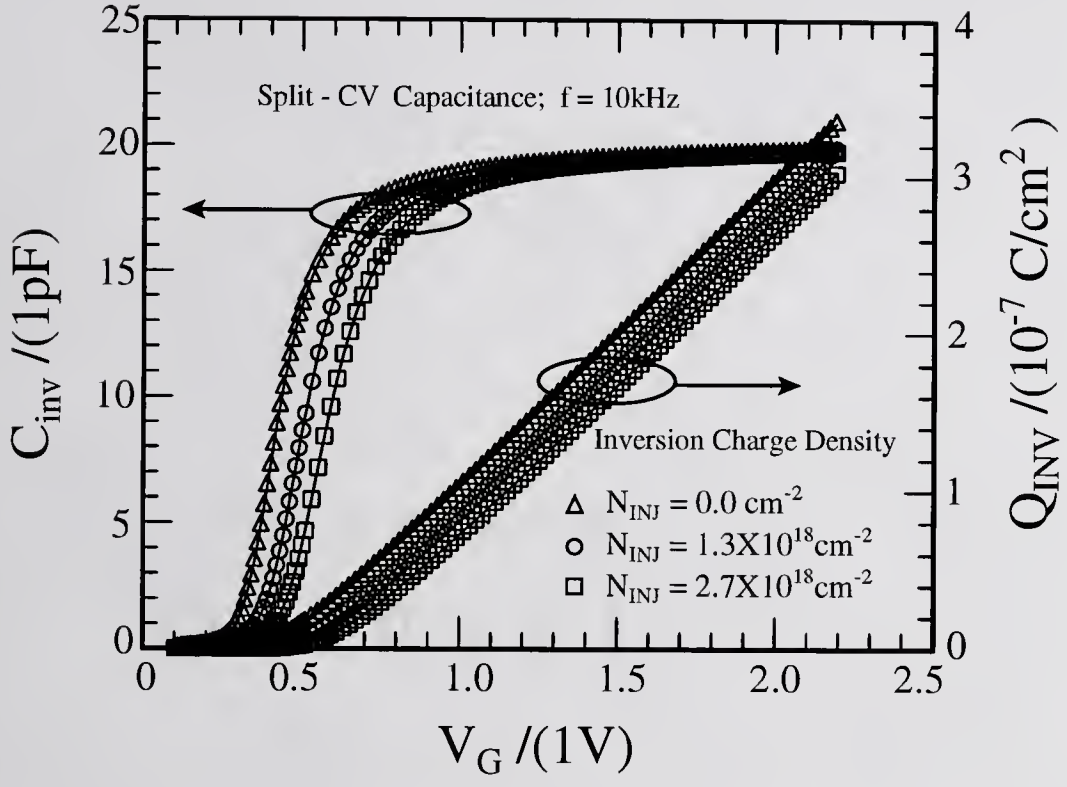



Figure 4.2 c Shift in the split-CV and $Q_{INV}$ of an n-channel BiMOST due to SHEi stress at a constant $E_{OX} = 4MV/cm$. The curves for three different fluences are plotted.

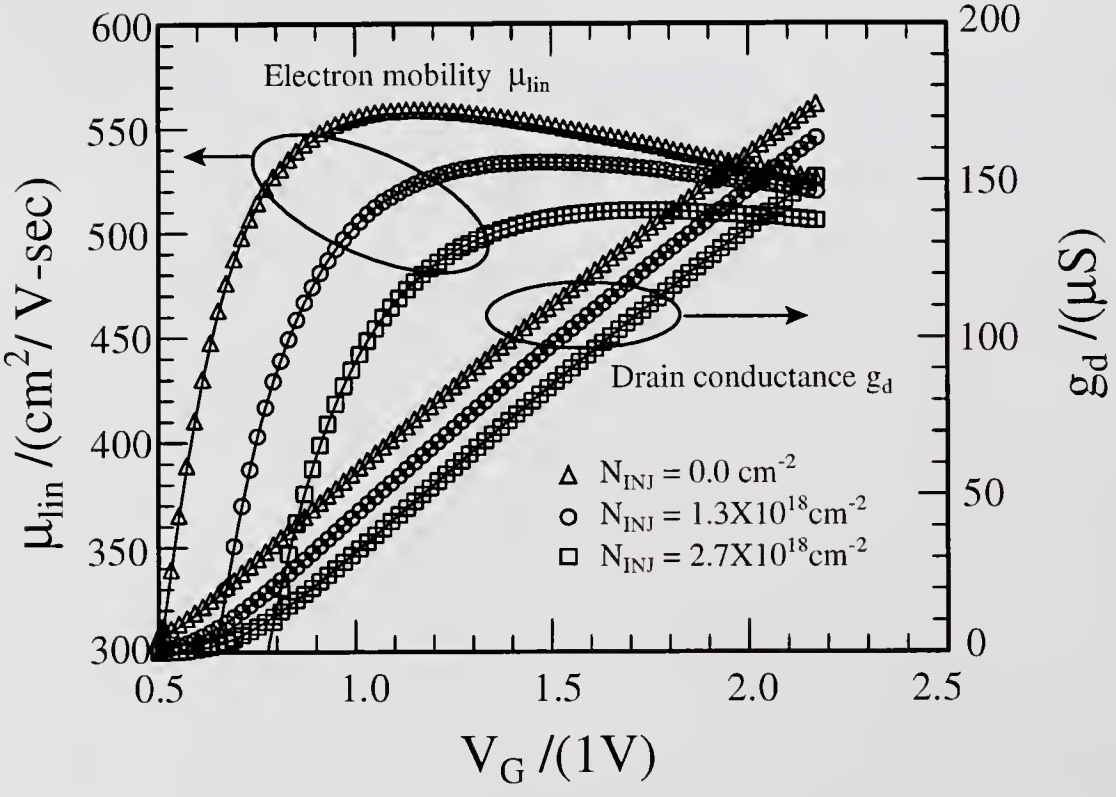



Figure 4.2 d Shift in the effective mobility and $g_d$ of an n-channel BiMOST due to SHEi stress at a constant $E_{OX}$ = 5MV/cm. The curves for three different fluences are plotted.

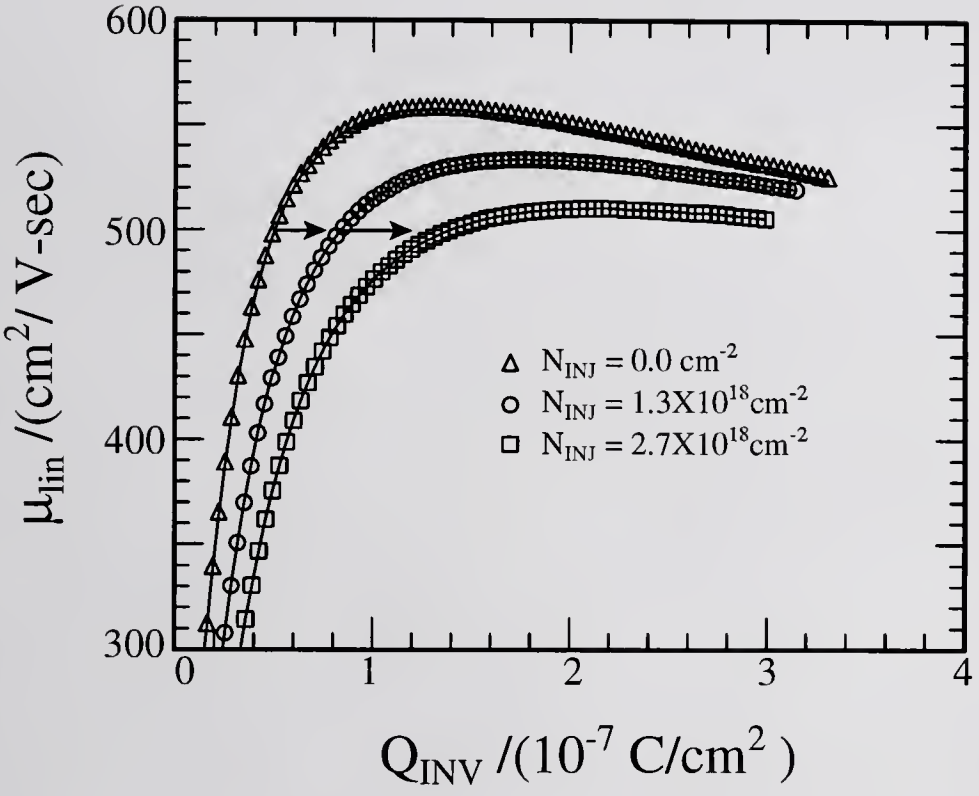



Figure 4.3a Shift in the effective mobility of an n-channel BiMOST due to SHEi stress at a constant $E_{OX}$ = 4MV/cm. The curves for three different fluences are plotted.

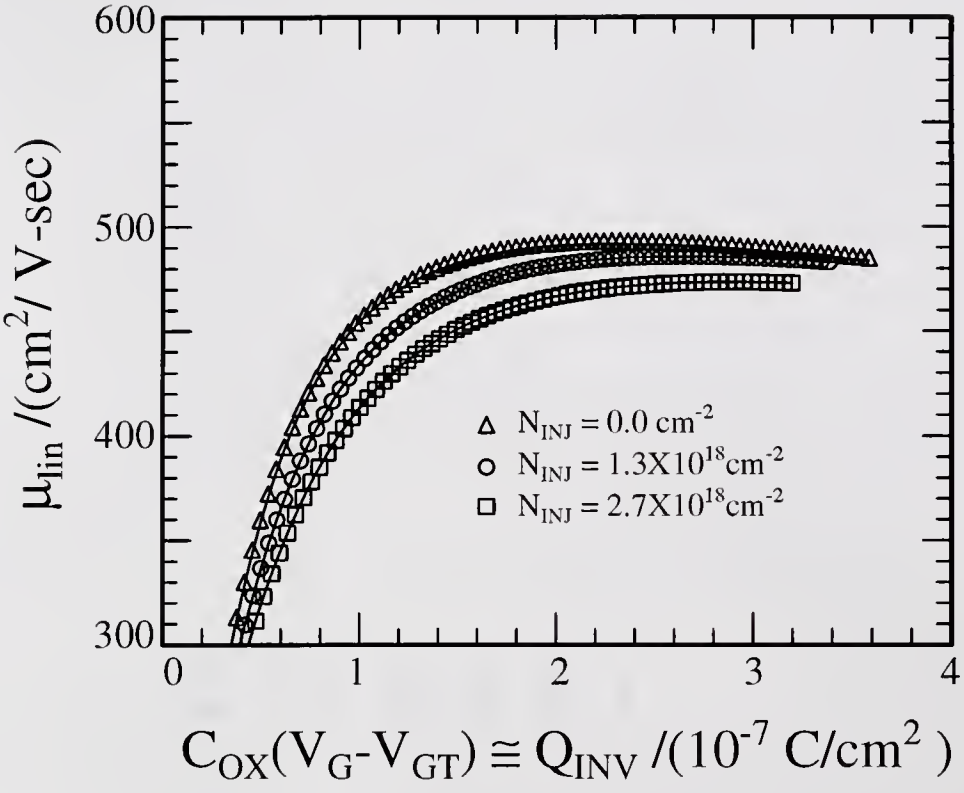



Figure 4.3 b Shift in the effective mobility of an n-channel BiMOST due to SHEi stress at a constant $E_{OX}$ = 4MV/cm. The curves for three different fluences are plotted versus an approximated $Q_{INV}$.

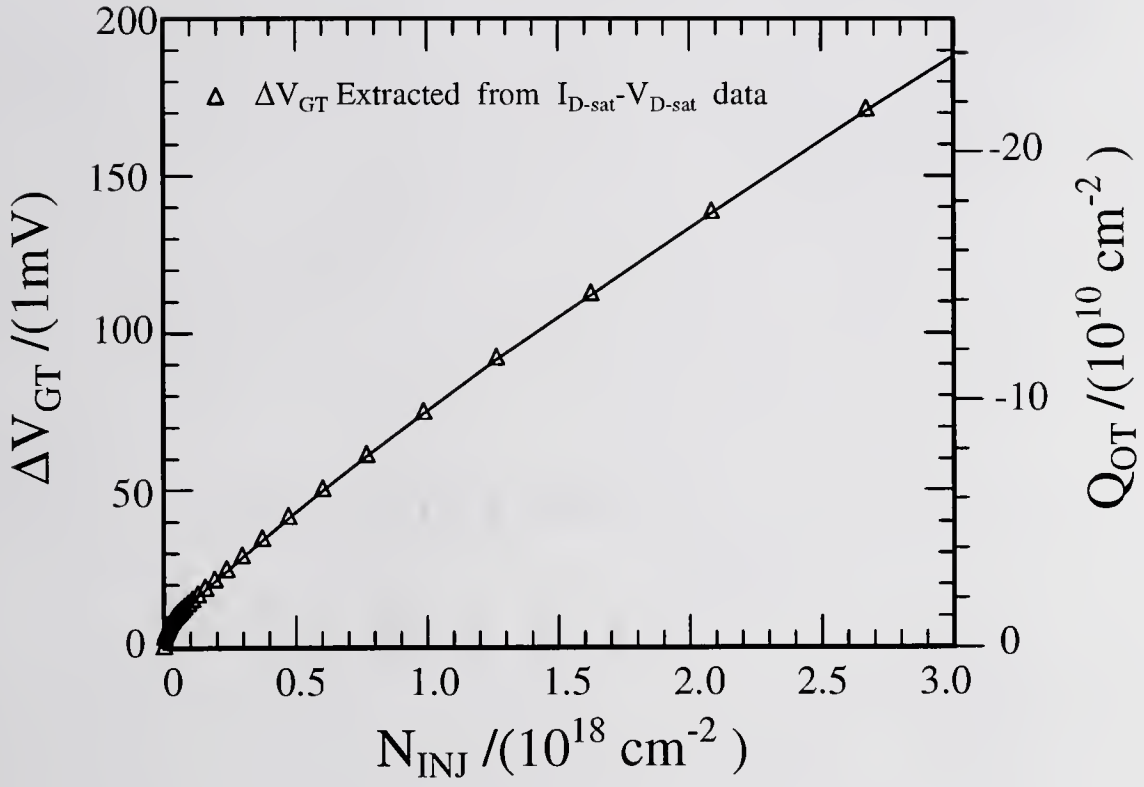



Figure 4.4 Threshold voltage shift of n-channel BiMOST during SHEi at T=295°K, $E_{OX}$= 4MV/cm, $V_{CB}$ = 4V and at a constant $I_G$=3nA.

time since the gate current sometimes varies from device to device. In Figure 4.5a and 4.5b the degradation of the saturation current, $\Delta I_{D\text{-}sat}$, is plotted versus the injection fluence, $N_{INJ}$. In Figure 4.5a the value of $I_{D\text{-}sat}$ is extracted at a constant value of $V_D = V_G > V_{D\text{-}sat} = V_G - V_{GT}$ whereas in Figure 4.5b $I_{D\text{-}sat}$ was extracted at $V_G - V_{GT}$; which includes the variation of $V_{GT}$ with $N_{INJ}$. Thus, Figure 4.5a illustrates the contributions to $\Delta I_{D\text{-}sat}$ from both the shift in the threshold voltage, $\Delta V_{GT}$, and the degradation or change of the saturation mobility $\Delta\mu_{sat}$ whereas Figure 4.5b $\Delta I_{D\text{-}sat}$ contains only the contributions of $\Delta\mu_{sat}$. The percent change in the effective saturation mobility, $\mu_{sat}$, and the effective conductivity or linear mobility, $\mu_{lin}$, versus the injection fluence is plotted in Figure 4.6. The value of $\mu_{lin}$ was monitored for a variety of constant $Q_{INV}$ values to maintain a constant surface field in the silicon. As clearly evident in Figures 4.3a and 4.3b, the mobility curves converge at large $Q_{INV}$ and hence the shift in $\mu_{lin}$ is less as shown in Figure 4.6. In Figure 4.6, the prestress values of $\mu_{lin}$ range from $557cm^2/V\text{-}sec$ near the peak of the curve at $Q_{INV}=1.34\times10^{-7}C/cm^2=8.4\times10^{11}q/cm^2$, to $532cm^2/V\text{-}sec$ at $Q_{INV}=2.51\times10^{-7}C/cm^2=1.57\times10^{12}q/cm^2$, while the prestress value of the effective saturation mobility is $518cm^2/V\text{-}sec$. Figure 4.6 indicates that the saturation mobility is more sensitive to the increasing charge in the oxide. To summarize the results, Figure 4.7 plots the extracted $\Delta V_{GT}$, $\Delta\mu_{lin}$, $\Delta\mu_{sat}$ versus the total $\Delta I_{D\text{-}sat}$ ($I_{D\text{-}sat}$ extracted $V_D = V_G = 1V$ = constant).

In order to quantify the effects of interface traps on the mobility, in addition to the just-described effects from the oxide charge buildup during the stress, two methods were employed to measure the increase in the interface trap's quantum density-of-state, $D_{IT}$. The first is the commonly used method of monitoring the change of the

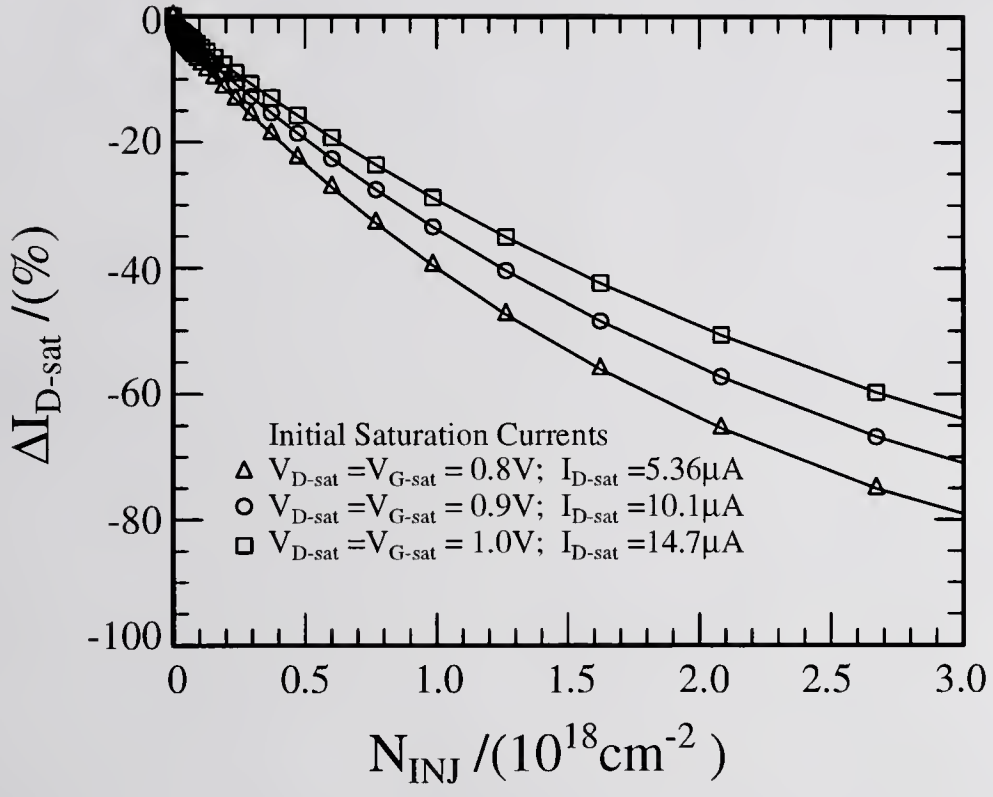



Figure 4.5 a Shift in the saturation current of an n-channel BiMOST due to SHEi stress at a constant $E_{OX}$= 4MV/cm. The value of $I_{D\text{-}sat}$ was extracted at a constant value of $V_{D\text{-}sat} = V_{G\text{-}sat}$.

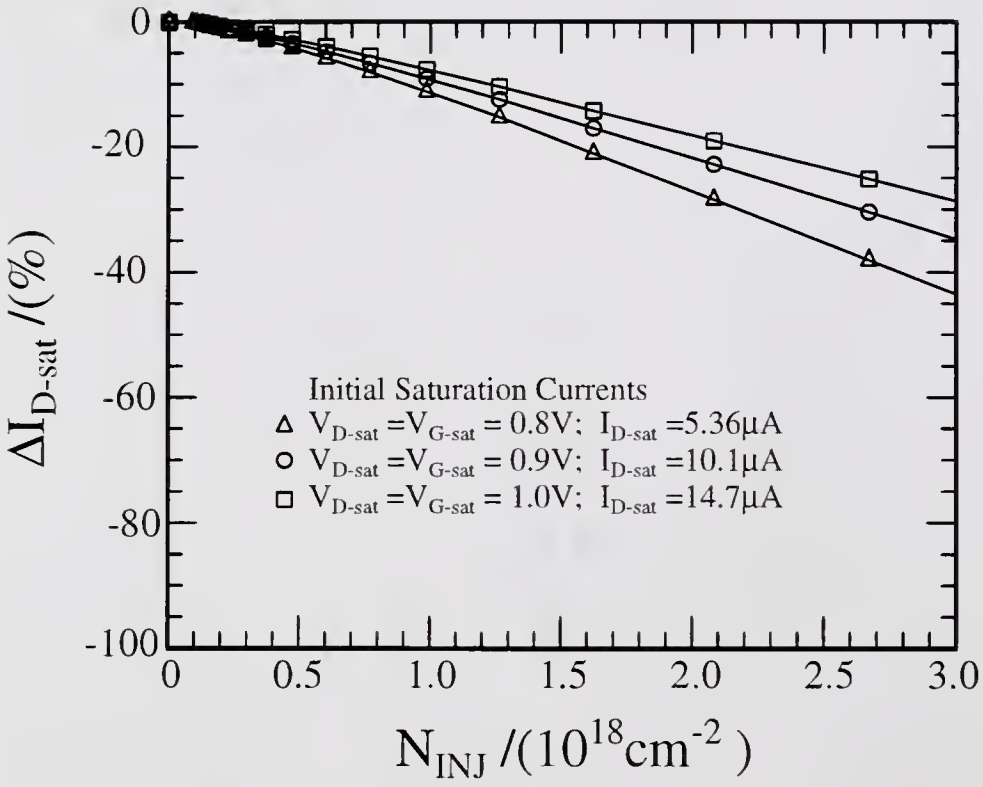



Figure 4.5 b Shift in the saturation current of an n-channel BiMOST due to SHEi stress at a constant $E_{OX}$= 4MV/cm. The value of $I_{D\text{-}sat}$ was extracted for a varying value of $V_{D\text{-}sat} = V_{G\text{-}sat}$ plus the extracted value of $V_{GT}$.

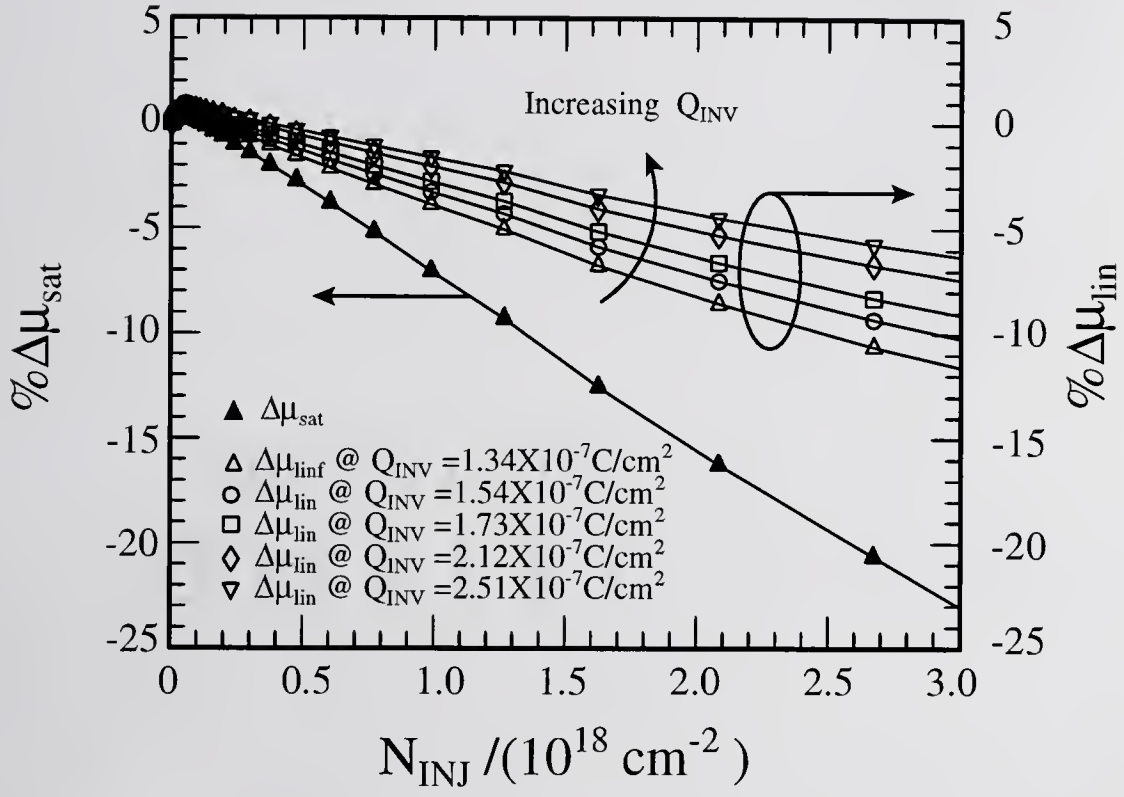



Figure 4.6 Percentage shift in the conductivity effective mobility, $\mu_{lin}$, for varying values of $Q_{INV}$, and in the saturation effective mobility, $\mu_{sat}$ plotted versus fluence for an n-channel BiMOST during SHEi stress at constant $E_{OX}$=4MV/cm and $V_{CB}$ = 4V.

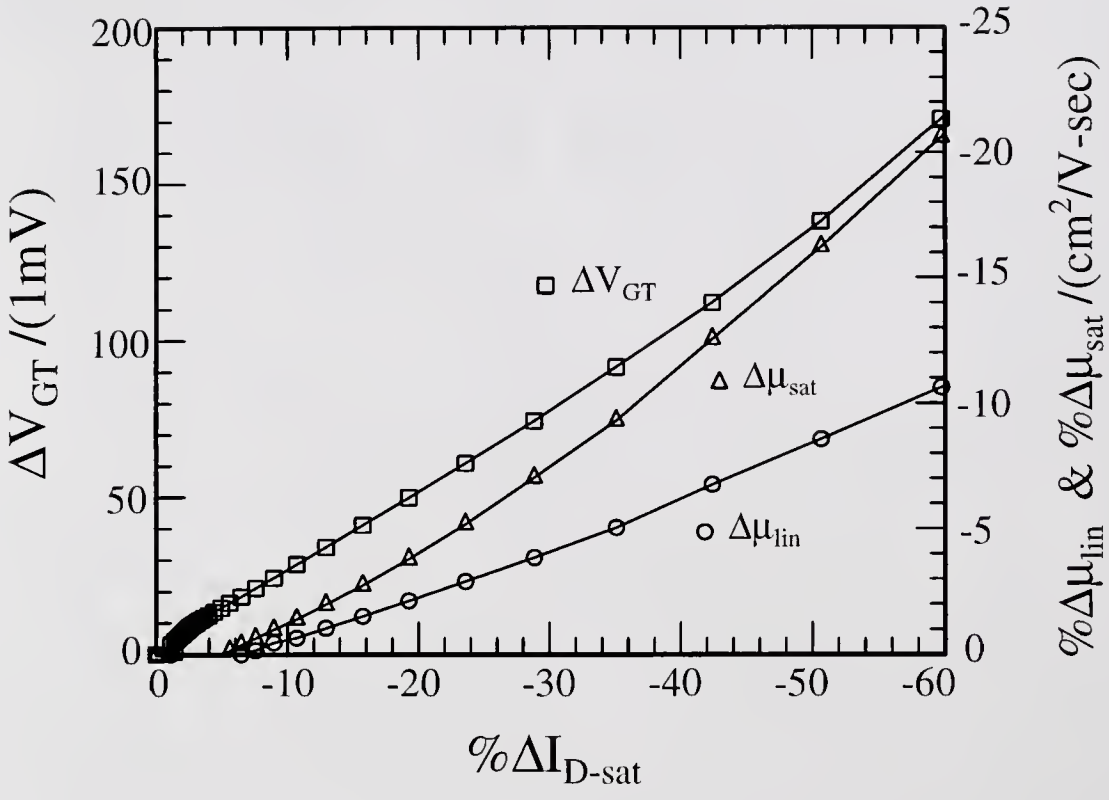



Figure 4.7 The relative change in threshold voltage, $V_{GT}$, the conductivity effective mobility, $\mu_{lin}$ and the saturation effective mobility, $\mu_{sat}$, versus the corresponding degradation in $I_{D\text{-}sat}$ for an n-channel. BiMOST stressed at $E_{OX} = 4MV/cm$.

subthreshold voltage swing, $\Delta S$, in which the inverse slope in the prestress subthreshold portion of the $I_D$-$V_{GS}$ data is measured and compared to that measured after each stress. Although the ideal theoretical value at room temperature is $\Delta V_G = 2.303 k_B T/q \approx 60mV$ per decade of $I_D$, a measured value of 80mV per decade is more common due to thick oxide and high substrate doping variation [10, Fig.682.1 on p.655]. The relation of the density of the generated interface trap to the subthreshold swing, $\Delta S$, is given by {See reference [10], Eqns.(683.10) and (683.11) on p.666.}

$$\Delta D_{IT} = D_{IT}(t_{stress}) - D_{IT}(0) = (C_{OX}/q)(q/2.303k_BT)\Delta S \ (\#/eV\text{-}cm^2). \qquad (4.2)$$

In our samples, the prestress density of interface traps is negligible and may be assumed zero,

$$\Delta S = S(D_{IT}) - S(D_{IT}=0) \approx S(D_{IT}). \qquad (4.3)$$

The second approach is a new method for measuring $D_{IT}$ buildup recently proposed by Neugroschel and Sah, and demonstrated by them and their graduate students [12]. This method takes advantage of the unique feature of the vertical bipolar junction transistor (BJT) structure in the BiMOST and the fact that the buildup of the BJT base recombination current, $\Delta I_B$, is directly and solely proportional to the buildup of the interface trap density because the additional recombination of the minority carriers (electrons in the p-base layer of n/p/n BJT of the nBiMOST) occurs at generated interface traps. They demonstrated the extraction of the interface trap density from the change of the stress-induced increase in the base current after each stress cycle. This new method was coined and acronymed by Sah as the so-called direct-current current-voltage measurement or DCIV.

The relationship between the change in the base current, $\Delta I_B$, the surface recombination velocity, $S_o$, and the emitter base bias, $V_{BE}$, is given by [12]

$$\Delta I_B \simeq (qAn_i\Delta S_0/2)\exp(qV_{BE}/k_BT) \tag{4.4}$$

$$\Delta S_0 \simeq (\pi/2)\sigma_0\Theta_{th}\Delta N_{IT} \tag{4.5}$$

where $\sigma_0$ is the cross-section of carrier capture at the interface traps, $\Theta_{th}$ is the carrier thermal velocity, and $\Delta N_{IT}$ is the stress-generated interface trap density (#/cm$^2$). The base current, $I_B$, versus the gate to base d.c. bias, $V_{GB}$, measured during the SHEi stress at $E_{OX}$=5MV/cm is shown in Figure 4.8 for three stress fluences, $N_{INJ}$ = 0, 1.3 and $2.7\times10^{18}$cm$^{-2}$. A comparison of the two measurements, $\Delta S$ and $\%\Delta I_B$, is shown in Figure 4.9 versus the injection fluence where %ΔIB/100 is calculated from,

$$\%\Delta I_B/100 = [I_B(t_{stress}) - I_B(0)]/I_B(0) \tag{4.6}$$

where $I_B(0)$ is the prestress value and $t_{stress}$ is the stress time or the stress fluence.

The results of the two interface trap monitoring methods indeed track each other quite well. The value for $D_{IT}$ plotted was calculated from $\Delta S$ assuming there are no interface traps in the unstressed sample. A calculation of $D_{IT}$ from $\Delta I_B$ would require an assumption for the cross-section, $\sigma_0$. In the following chapter a more thorough comparison of $\Delta S$ with $\Delta I_B$ will be given to separate the effects of interface traps and areal (y-direction) nonuniformity of trapped oxide charge.

In order to investigate the effect of different charge distributions within the oxide (x-direction) another device from the same 170Å group was stressed at a lower gate oxide electric field of 4MV/cm with all other stress and characterization parameters remaining the same. Minority carriers traveling through the gate oxide during the SHEi will now have a lower kinetic energies and will give a different oxide charge

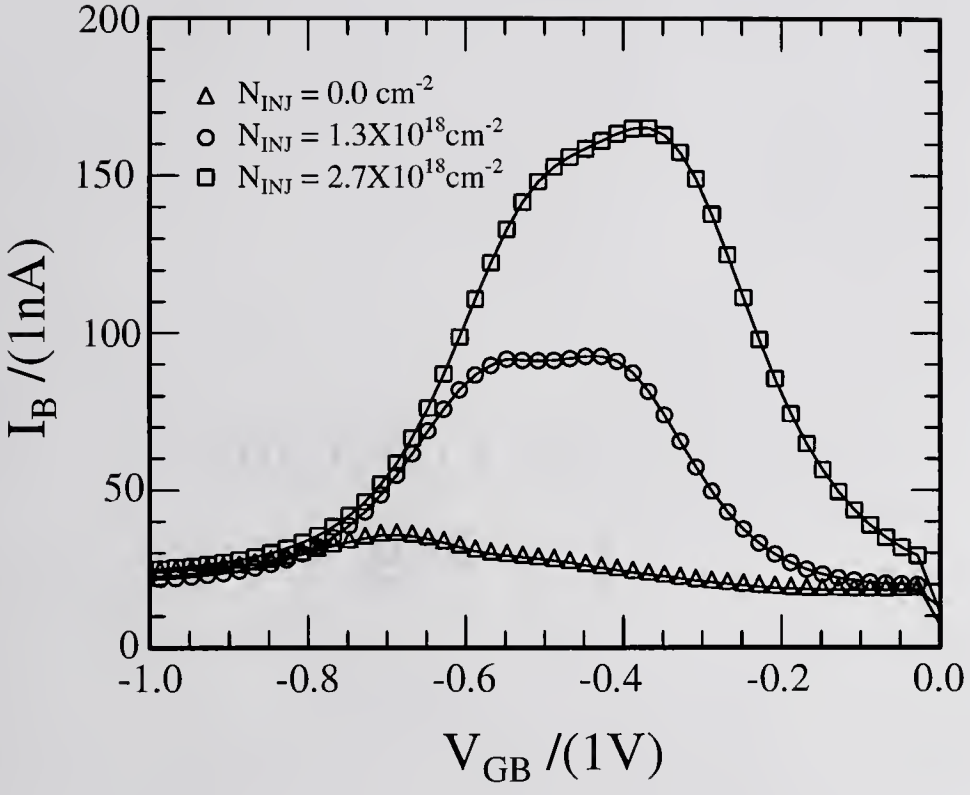



Figure 4.8 Increase of the base current of an n-channel BiMOST due to the build-up of interface states during SHEi stress at a constant $E_{OX}$=4MV/cm. $I_B$ is plotted for three different fluences.

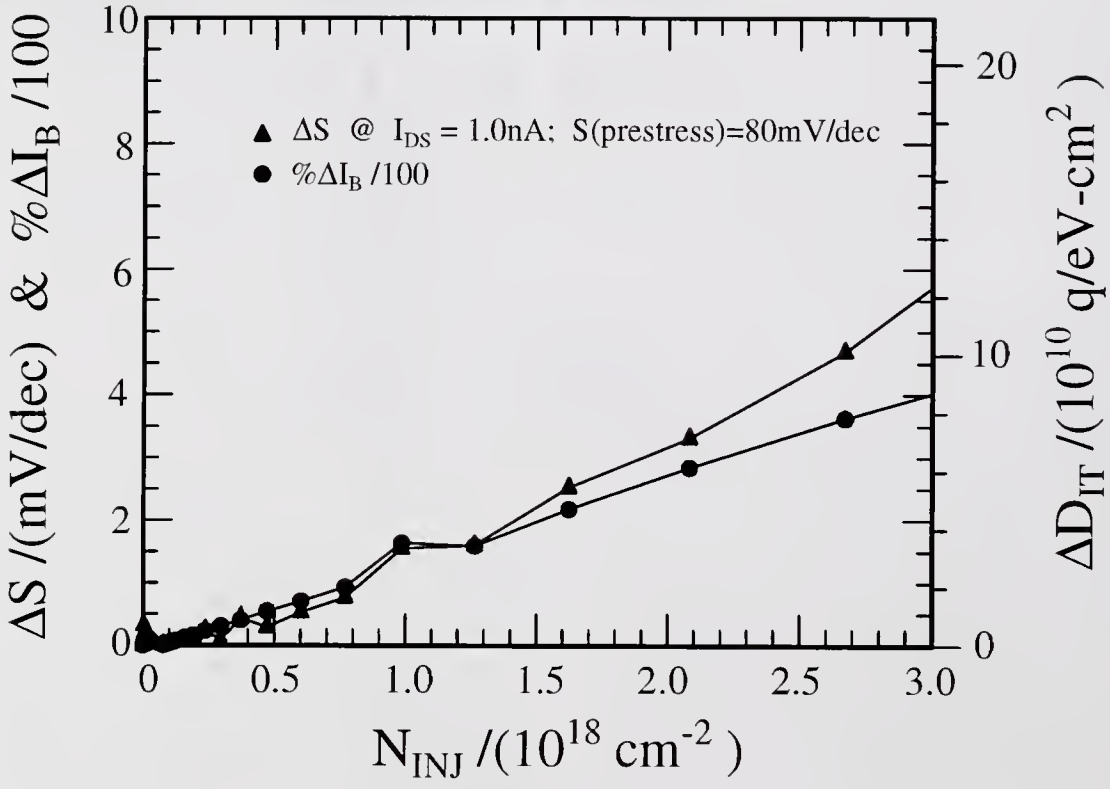



Figure 4.9 Shift in the subthreshold slope, S, and the corresponding increase in the base current, $\Delta I_B$, of an n-shannel BiMOST due to the the build-up of interface states during SHEi stress at a constant $E_{OX}$=4MV/cm.

distribution in the thickness direction or x-direction of the thin gate oxide film, $Q_{OT}$ = $Q_{OT}(x)$. Furthermore, the lower electric oxide field of 4MV/cm will give a lower field-aided and tunneling emission rates of electrons trapped in shallow energy levels in the oxide. Figures 4.10-4.14 give an illustration of the oxide electric dependence of the stress induced $\Delta V_{GT}$, $\Delta I_{D\text{-}sat}$, $\Delta\mu_{lin}$, $\Delta\mu_{sat}$, $\Delta S$ and $\Delta I_B$ versus fluence for $E_{OX}$=3MV/cm and $E_{OX}$=4MV/cm. The degradation of all these parameters indeed increases with increasing gate oxide electric field. Furthermore the lower field stress appears to cause a saturation of these parameters at a lower fluence, indicating that the oxide trap charging or discharging rate may be lower and that the traps being filled by or emptied of electrons have a larger capture or emission cross-section. In order to make a fair comparison of the degradation in the extracted $\Delta\mu_{lin}$ and $\Delta\mu_{sat}$ at the two gate oxide electric fields, Figure 4.12 should be replotted versus the trapped charge density, $Q_{OT}$. Hence if the spatial distribution (in x-direction or the oxide-thickness direction) of the stress built-up oxide traps at different $E_{OX}$ and stress conditions were the same, the degradation in the two effective mobilities would be the same. However, the two mobilities and drain current are also degraded and the gate threshold voltage is also changed by the stress-generated interface traps which cannot be reversed during the electronic neutralization of the oxide traps by electron thermal capture and tunnel emission, because the generated interface traps cannot be removed or annealed electronically. The two experiments described in the next two subsections will demonstrate the reversibility of $\mu_{lin}$, $\mu_{sat}$, $I_{D\text{-}sat}$, and $V_{GT}$ during the positive and negative charging and neutralization cycles of the oxide traps.

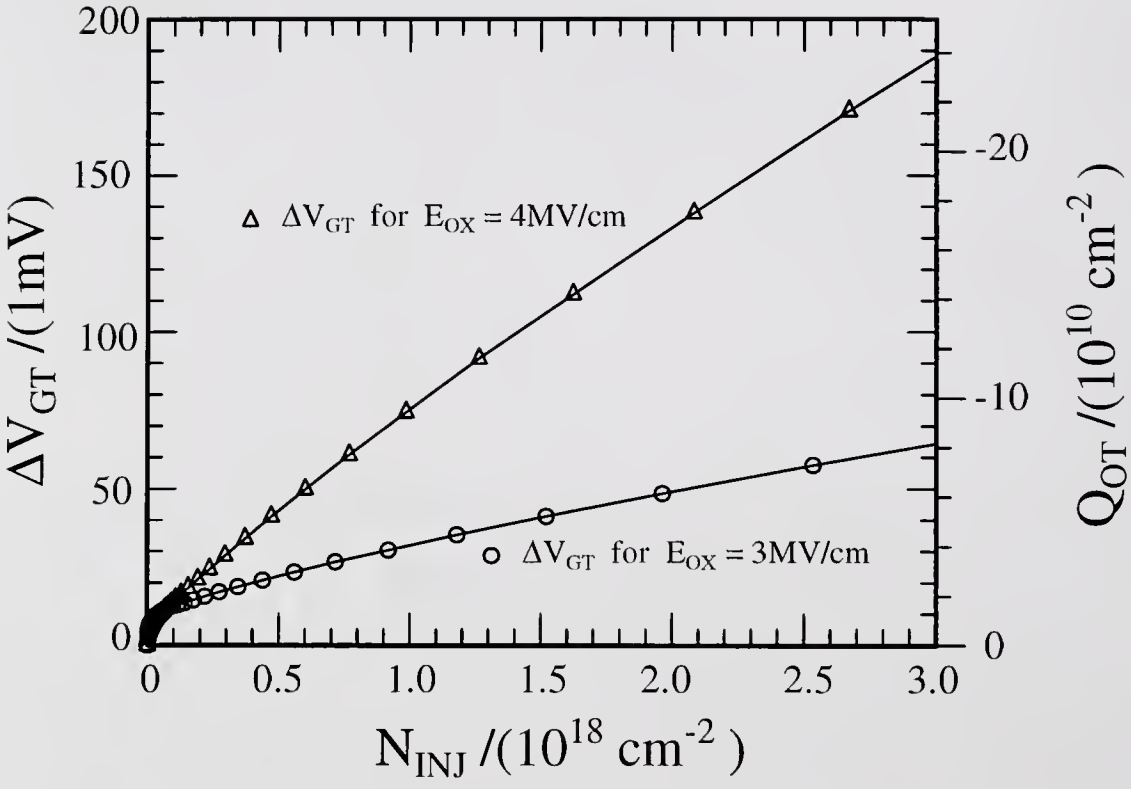



Figure 4.10 Threshold voltage shift of n-channel BiMOST during SHEi at $E_{OX}$=3MV/cm and $E_{OX}$=4MV/cm; $V_{CB}$=4V; T=295°K.

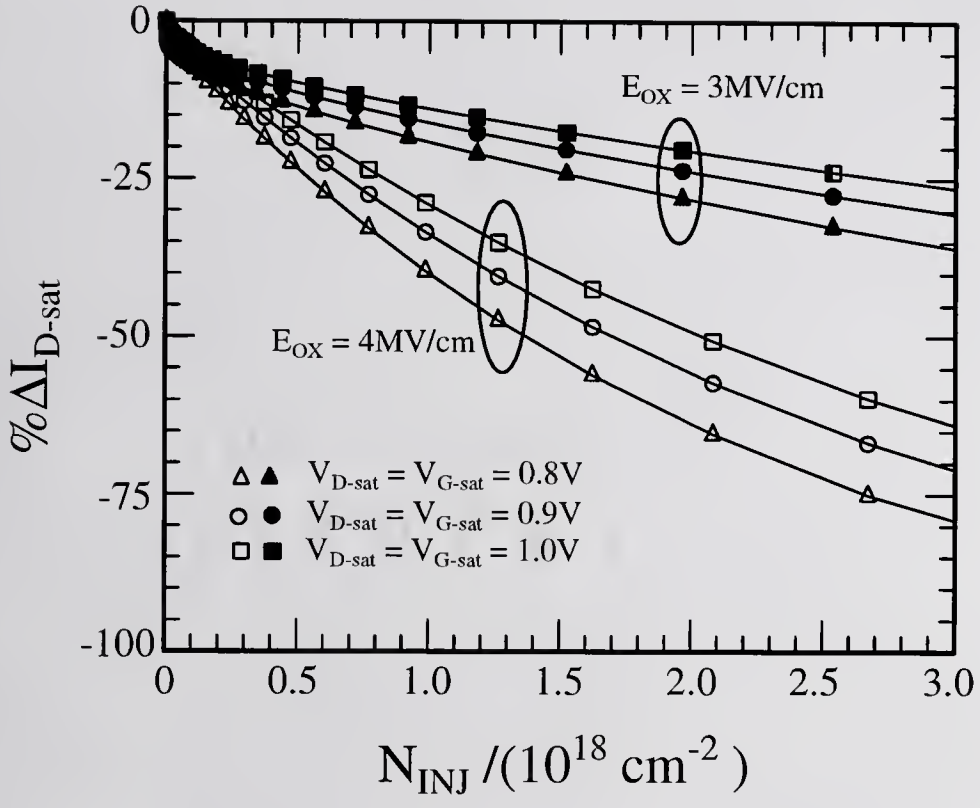



Figure 4.11a Shift in the saturation current of an n-channel BiMOST due to SHEi stress at $E_{OX}$=3MV/cm and $E_{OX}$=4MV/cm. The value of $I_{D\text{-}sat}$ was extracted at a constant value of $V_{D\text{-}sat}$= $V_{G\text{-}sat}$..

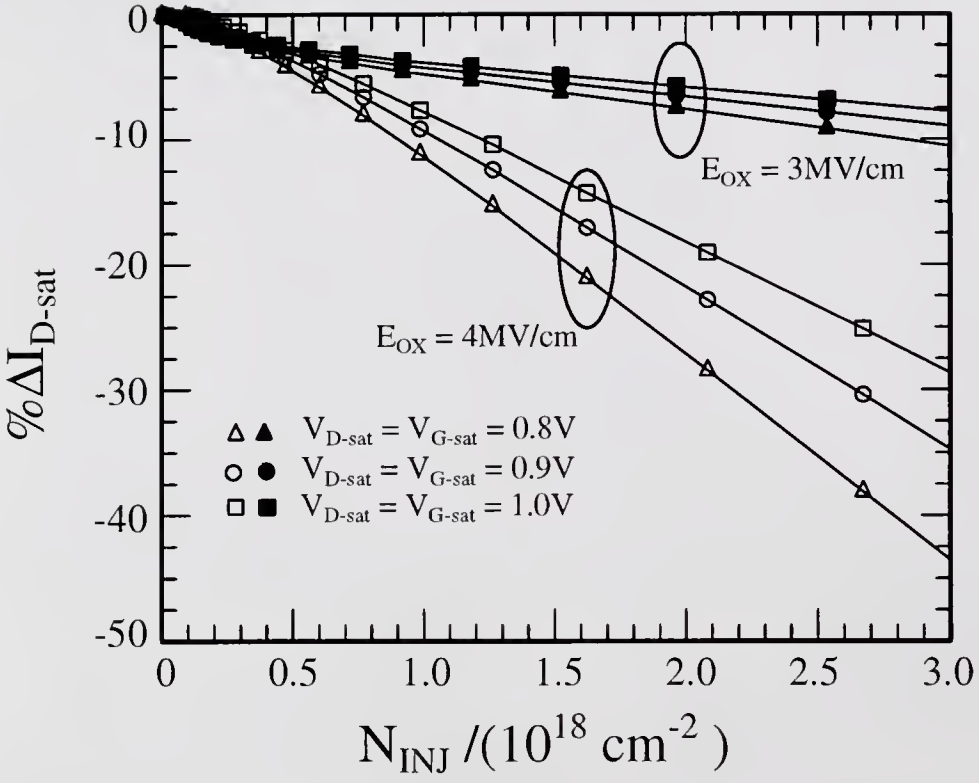



Figure 4.11 b Shift in the saturation current of an n-channel BiMOST due to SHEi stress at $E_{OX}$=3MV/cm and $E_{OX}$=4MV/cm. The value of $I_{D\text{-}sat}$ was extracted for a varying value of $V_{D\text{-}sat}$= $V_{G\text{-}sat}$. plus the extracted value of $V_{GT}$

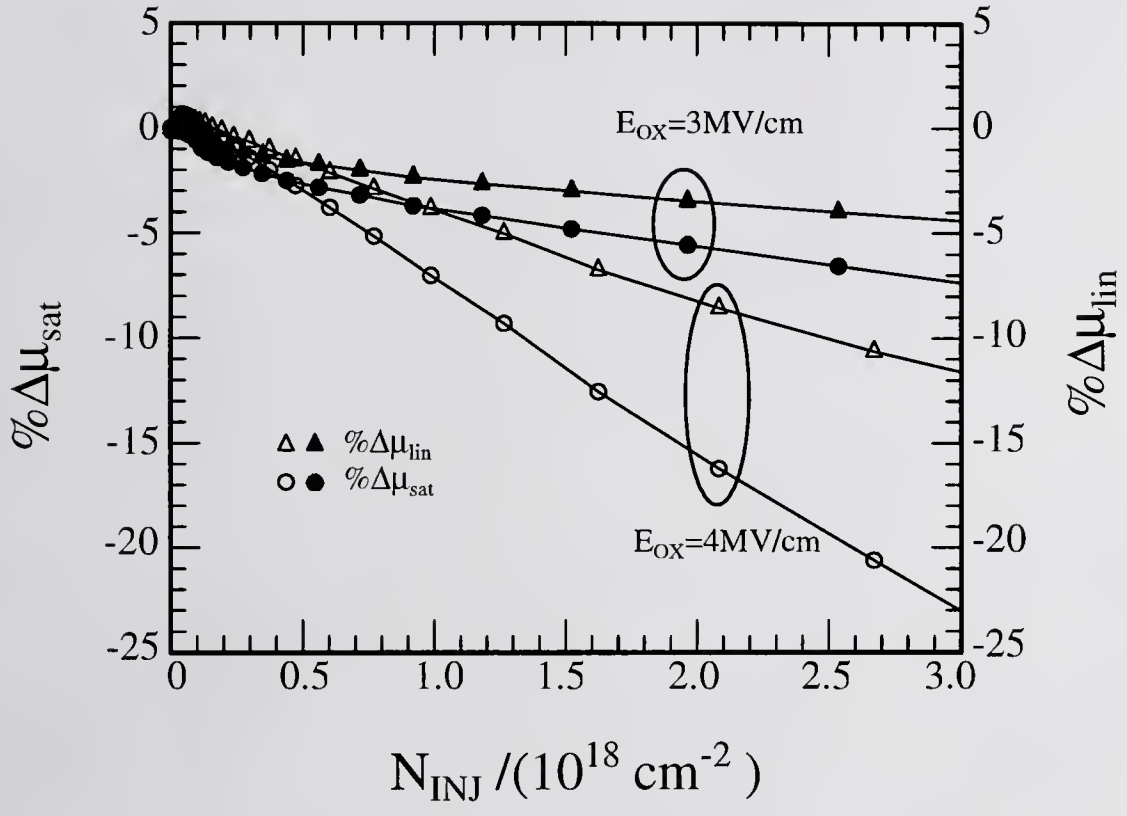



Figure 4.12 Percentage shift in the conductivity effective mobility, $\mu_{lin}$ and saturation effective mobility, $\mu_{sat}$ of electrons plotted versus fluence for an n-channel BiMOST during SHEi stress at $E_{OX}$=3MV/cm and $E_{OX}$=4MV/cm and $V_{CB}$=4V.

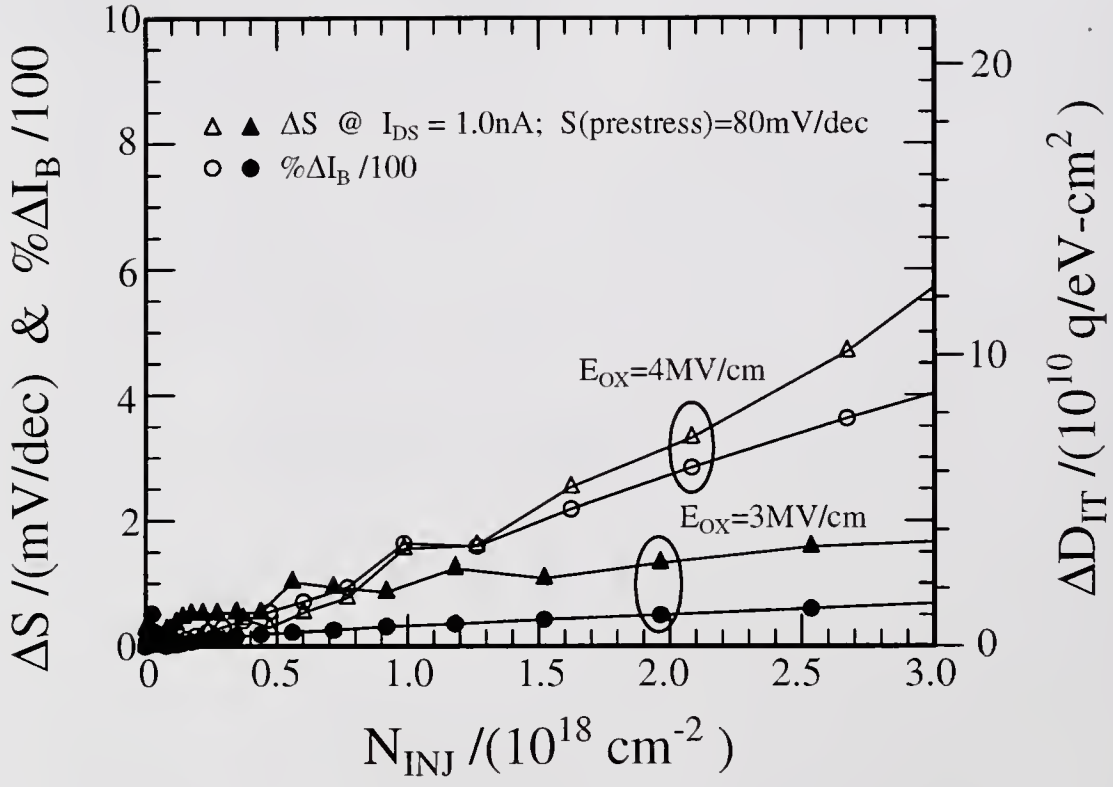



Figure 4.13 Shift in the subthreshold slope, S, and the corresponding increase in the base current, $\Delta I_B$, of an n-shannel BiMOST due to the the build-up of interface states during SHEi stress at a constant $E_{OX}$=3MV/cm and $E_{OX}$=4MV/cm and $V_{CB}$=4V.

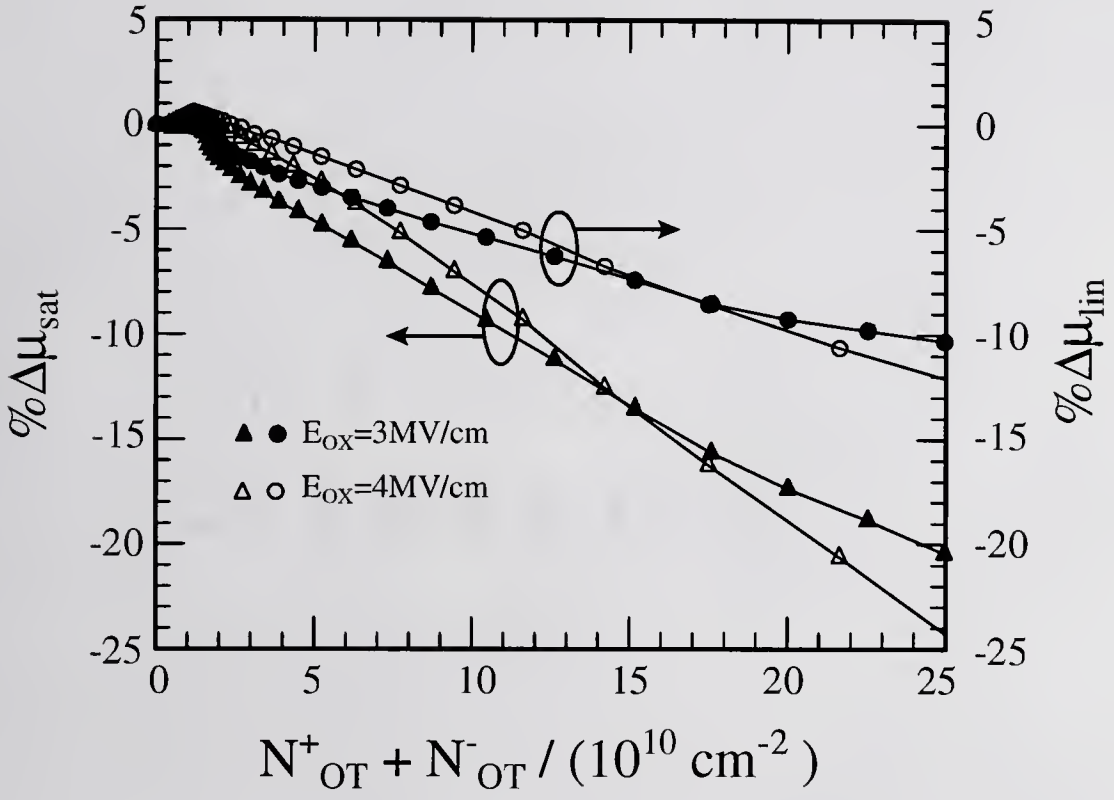



Figure 4.14 Percentage shift in the conductivity effective mobility, $\mu_{neff}$ and saturation effective mobility, $\mu_{nsat}$ of electrons plotted versus the net trapped charge density for an n-channel BiMOST during SHEi stress at $E_{OX}$=3MV/cm and $E_{OX}$=4MV/cm; $V_{CB}$=4V.

## 4.2 Charging and discharging the deep oxygen vacancy center at $E_C - 7eV$

One of the recently identified and studied defects in the $SiO_2$ quartz, optical fibers, and MOST's gate oxide is the E' center, commonly known as the bridging oxygen vacancy center, pictured in Figure 4.15. The chemical symbol to be used in this thesis will be $V_O$ for the bridging oxygen vacancy center, and $V_O^+$, $V_O^0$, and $V_O^-$ for the center in the three charged states as proposed by Sah to account for the electronic transitions between the multi-charge-states of the oxygen vacancy center [54, Fig.B3.4 on page 422.]. Thompson [56, 57] monitored the buildup kinetics of positive charge in the oxide during FNTE or SHE injection stress at high oxide electric fields (Fig. 4.15c). His findings were attributed by Sah to the bridging oxygen vacancy [54, Fig.B3.4 on page 422.]. The E' center has been well known in fiber and optical glass investigations and its microscopic configuration indicated in Figure 4.15d was delineated by electron paramagnetic resonance spectroscopy [58]. It is but only one of the charge state configurations of the oxygen vacancy center, that is detectable by spin resonance of an unpaired electron. The multi-charge-state and transition energy band model proposed by Sah, as depicted in Figure 4.15c, suggests that positive oxide charge is created when one of the bound electrons at an initially neutral oxygen vacancy site $[(Si\text{-}O)_3{\equiv}Si^{\cdot}Si{\equiv}(O\text{-}Si)_3]$, is impact emitted or released by an energetic electron (kinetic energy > 7eV). In Thompson's experiment suggested by Sah, electrons were injected into the gate oxide from the gate electrode during FNTEi or from the substrate during SHEi. They were then accelerated to 7eV by the oxide electric field to gain sufficient kinetic energy to impact release the bond electron at the

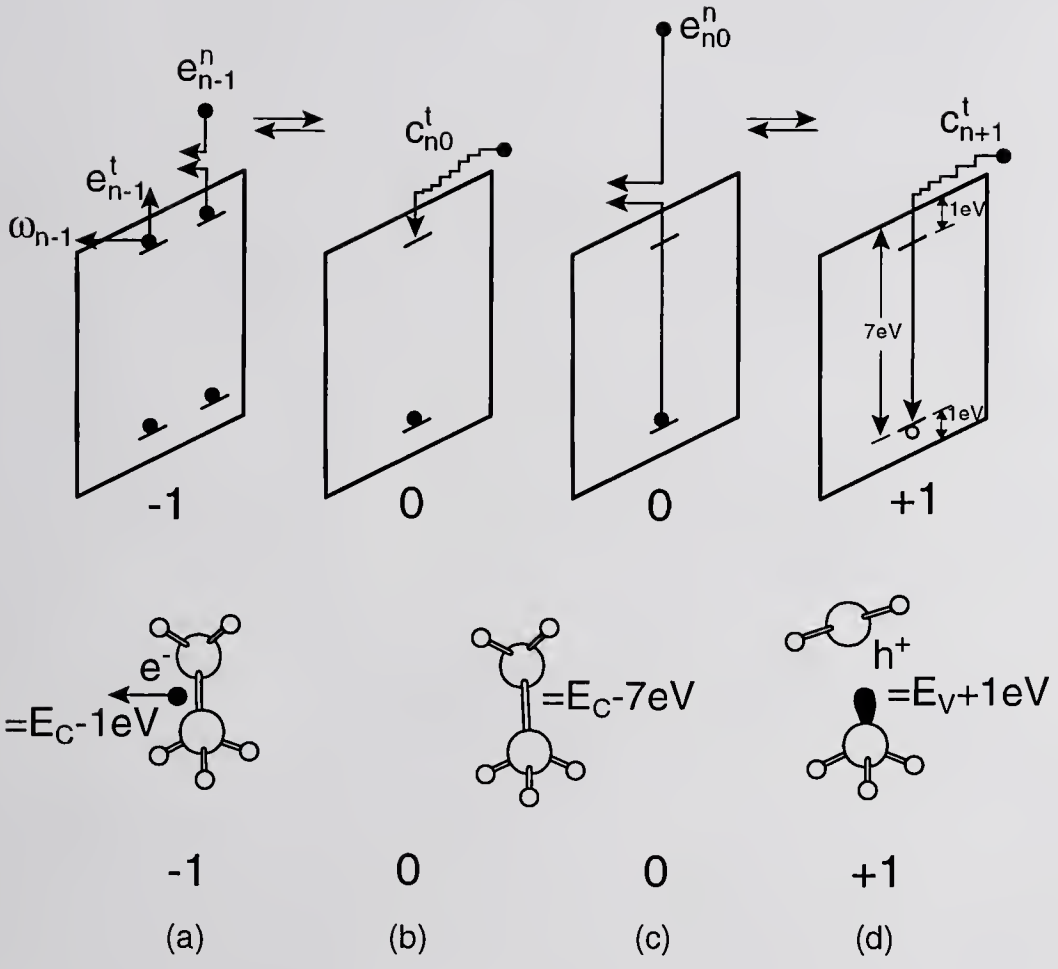



Figure 4.15 Energy band diagram illustrating the various states of the E' center otherwise known as the oxygen vacancy; (a) thermal or tunneling emission from a shallow state, (b) thermal capture at a shallow state, (c) generation of positive charge by impact emission of a bound electron by an energetic electron injected from the substrate or poly-gate, and (d) thermal capture at the deeper level ($E_C$-$E_t$=7eV) [51, Fig. B3.4]

neutral oxygen vacancy. These positively charged oxygen vacancy centers can then be neutralized by capturing electrons (Fig. 4.15d) from low-field SHEi, at sufficiently low oxide electric field such that the kinetic energy gained by injected electrons in the oxide is less than about 7eV and impact emission of the newly captured electrons would be avoided.

The results of charging and discharging the 7eV oxygen vacancy center under high and low oxide electric fields and the effect of charge on the electron mobility and $I_{D\text{-}sat}$ will now be discussed. An n-channel BiMOST ($X_{OX}$=170Å) was first subjected to the low field $E_{OX}$=1.5MV/cm SHEi stress to fill any already positively charged states in the oxide. The positive threshold voltage shift, $\Delta V_{GT}$, is shown in Figure 4.16a and enlarged in Figure 4.16b at low fluence ($N_{INJ}<4X10^{14}/cm^2$). Next electrons were Fowler-Nordheim tunnel injected from the poly-gate into the oxide to impact emit the trapped electrons from the $E_C - 7eV$ level of the $V_O^0$ center in the oxide giving $V_O^0 + e^{-*} \rightarrow V_O^+ + 2e^-$. The resulting negative threshold voltage shift is illustrated in Figure 4.16a. Finally the oxide was again SHE injected at $E_{OX}$=1.5MV/cm to refill the positively charged centers, $V_O^+ + e^- \rightarrow V_O^0$, as indicated in the enlargement of Figure 4.16c for ($9\times10^{15} < N_{INJ} < 9.4\times10^{15}cm^{-2}$). Clearly $V_{GT}$ recovers almost completely, to within 10mV of the initial value after low-field SHEi.

In Figures 4.17 and 4.18 the corresponding $\Delta I_{D\text{-}sat}$ are shown. The value of $I_{D\text{-}sat}$ was extracted at a constant $V_D=V_G$ in Figure 4.17 and at $V_D=V_G$ adjusted by $\Delta V_{GT}$ in Figure 4.18 to separate the mobility and threshold voltage contributions to $\Delta I_{D\text{-}sat}$. These two figures differ drastically due to the fact that the built-up oxide charge does not seem to affect the value of $\mu_{sat}$ as much as $V_{GT}$. Therefore the degradation

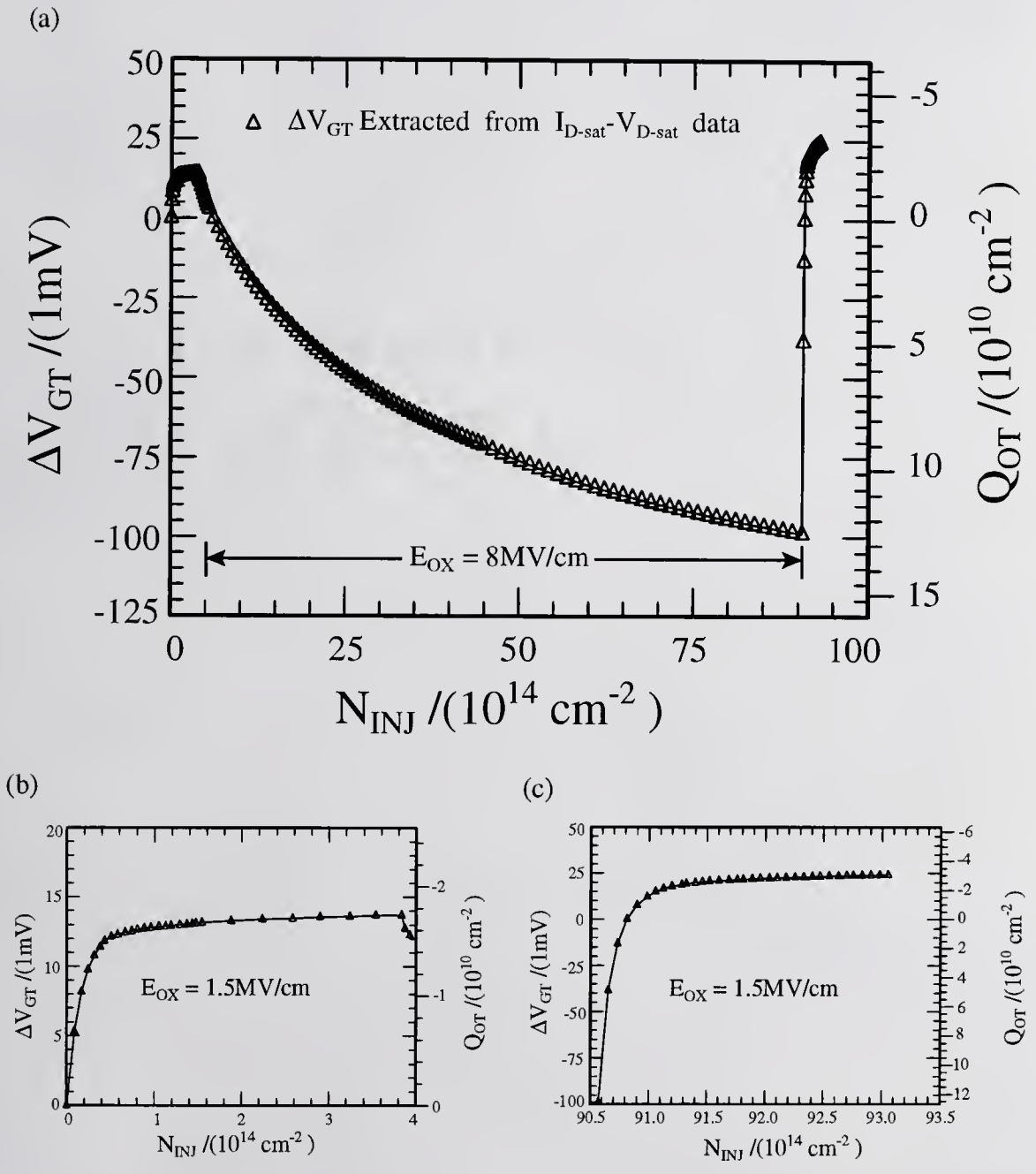



Figure 4.16 (a) Threshold voltage shift of n-channel BiMOST during SHEi at $E_{OX}$= 1.5MV/cm enlarged in (b) for $N_{INJ}$<4 x$10^{14}$, followed by FNTEi from the gate at $E_{OX}$ = 8MV/cm, for 4 x$10^{14}$< $N_{INJ}$< 9 x$10^{15}$ ,and again by SHEi at $E_{OX}$=1.5MV/cm for 9 x$10^{15}$< $N_{INJ}$< 9.4 x$10^{15}$ enlarged in (c).

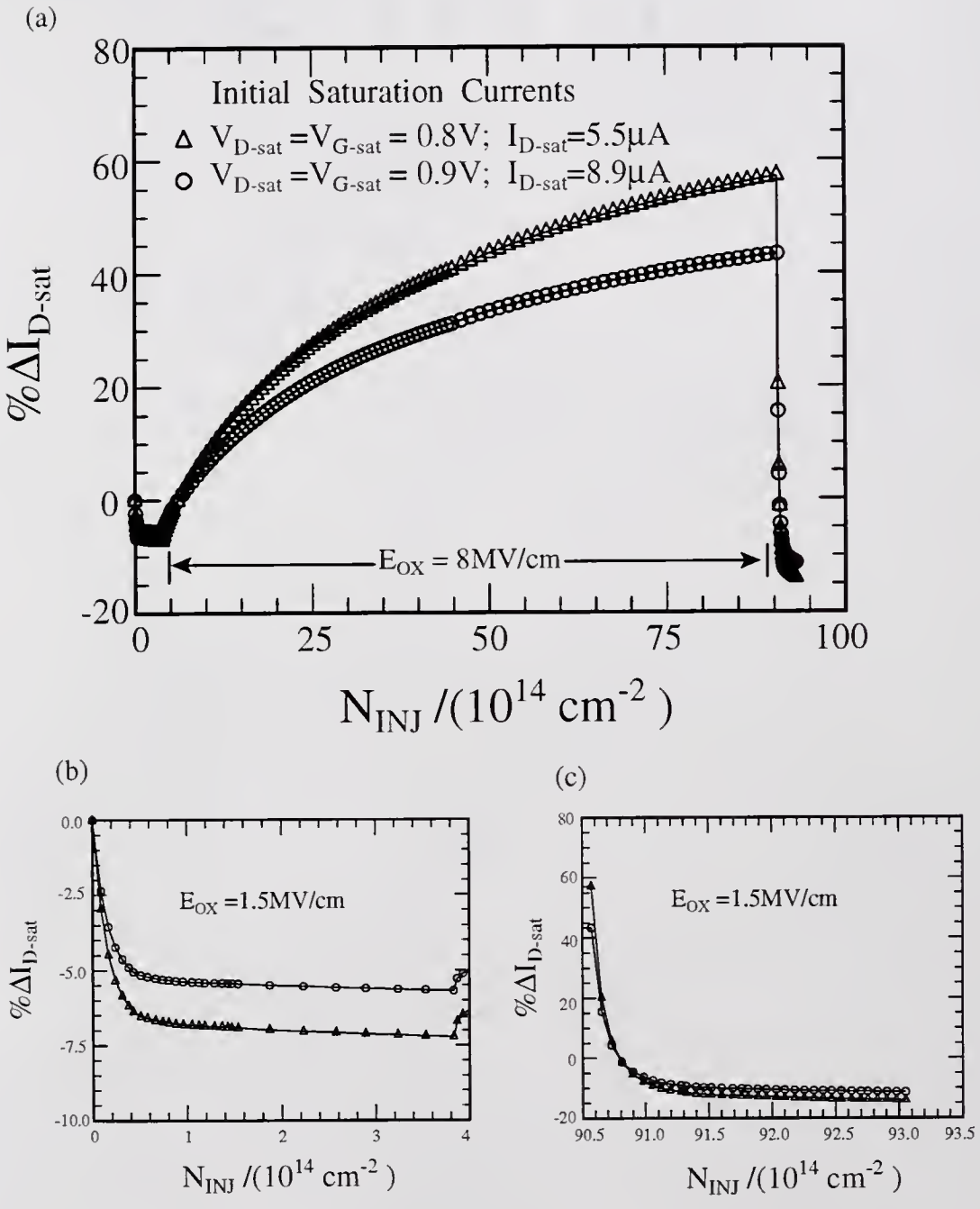



Figure 4.17 Shift in the saturation current of an n-channel BiMOST during SHEi at $E_{OX}$=1.5MV/cm enlarged in (b) for $N_{INJ}$<4 x$10^{14}$, followed by FNTEi from the poly-gate at $E_{OX}$=8MV/cm, for 4 x10<$N_{INJ}$<9 x$10^{15}$ and again by SHEi at $E_{OX}$=1.5MV/cm for 9 x$10^{15}$<$N_{INJ}$<9 x$10^{15}$ in (c).

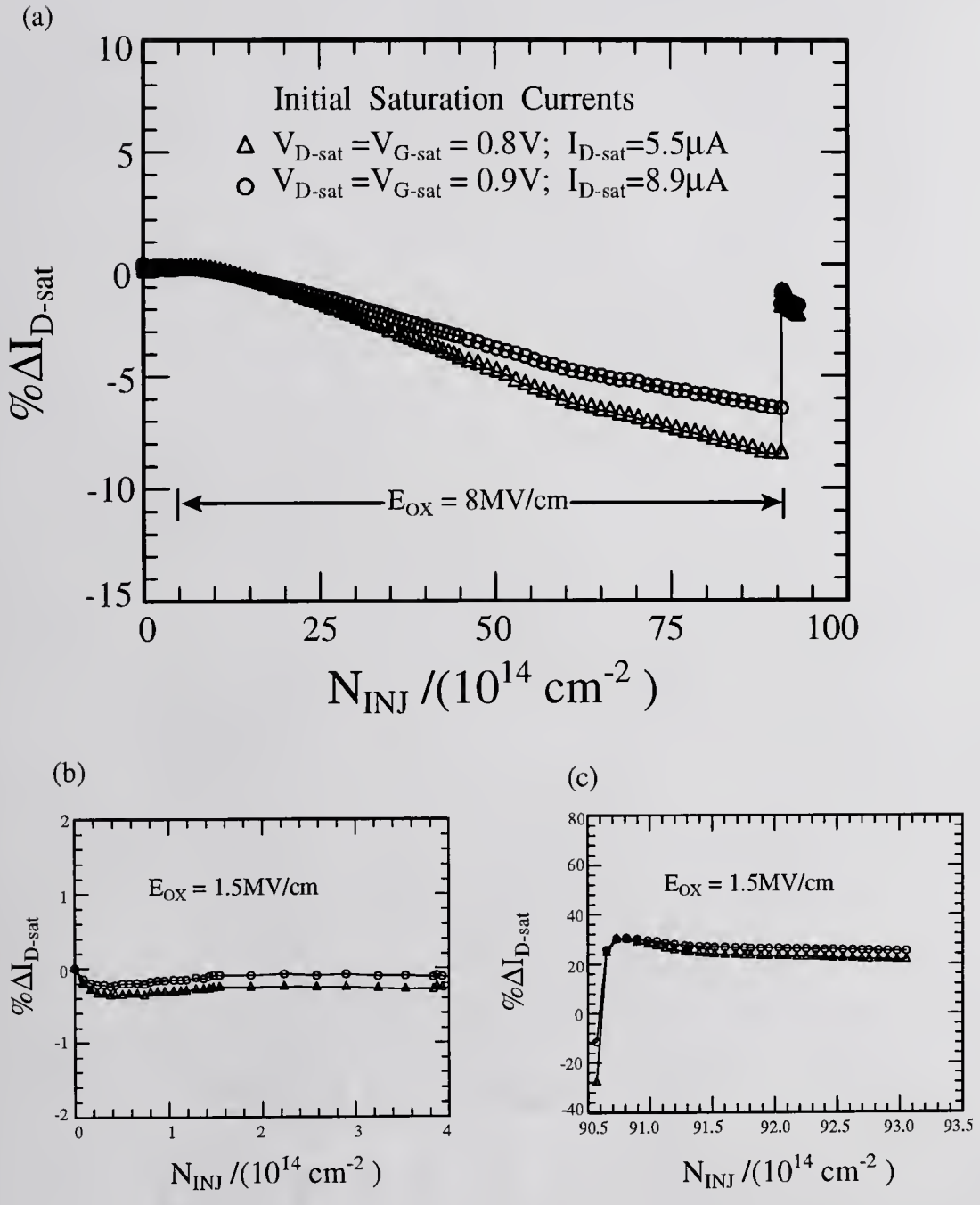



Figure 4.18 Shift in the saturation current of an n-channel BiMOST during SHEi at $E_{OX}$=1.5MV/cm enlarged in (b) for $N_{INJ}$<4 x$10^{14}$, followed by FNTEi from the poly-gate at $E_{OX}$=8MV/cm, for 4 x10<$N_{INJ}$<9 x$10^{15}$ and again by SHEi at $E_{OX}$=1.5MV/cm for 9 x$10^{15}$<$N_{INJ}$<9 x$10^{15}$ in (c). The value of $I_{D\text{-}sat}$ was extracted at a constant $V_{D\text{-}sat}$=$V_{G\text{-}sat}$ plus $\Delta V_{GT}$.

in $I_{D\text{-}sat}$ appears negligible if the value of $V_D=V_G+\Delta V_{GT}$ is used to extract the current as in Figure 4.18. This figure essentially illustrates $\Delta I_{D\text{-}sat}$ due to the degradation in mobility. This is also evident in the plot of the mobility degradation in Figure 4.19. The three hollow marker curves in this plot give $\mu_{lin}$ extracted at at three constant values of $Q_{INV}$. These curves support my assumption that the positively charged oxygen vacancy, $V_O^+$, are filled with electrons during the low field SHEi to neutralize the centers, decrease the Coulombic scattering, and increase the mobility, as I anticipated in designing this set of experiments. On the other hand during the high field FNTEi the electrons are impact emitted from the 7eV level leaving behind a positively charged center. This in turn increases the Coulombic scattering and decreases $\mu_{lin}$. The solid triangle curve in Figure 4.19 represents the saturation mobility, $\mu_{sat}$, which appears to be less sensitive to charging and discharging of this oxide trap (oxygen vacancy) as suggested by the difference between Figures 4.17 and 4.18. Thompson showed [56] that the centroid for this positive charge, $V_O^+$, is approximately 80-90Å from the injecting interface or at about central plane of the 170Å oxide layer investigated here. Nevertheless $\mu_{sat}$ does degrade slightly during the long FNTEi impact emission cycle and does recover immediately following the start of the second low field SHEi cycle. By isolating the initial portion of the high-field FNTEi and plotting the extracted positive oxide charge density, $+Q_{OT} = -(C_{OX}/q)\Delta V_{GT}$, against the degradation of $\mu_{lin}$ (at a constant $Q_{INV}=1.5\times10^{-7}C/cm^2=9.4\times10^{11}q/cm^2$) an essentially linear dependence on the oxide charge, $Q_{OT}$, is revealed (Fig. 4.19d).

Finally it is noted that the generation of interface states as measured by $\Delta S$ and $\Delta I_B$ was negligible during the SHEi portions of the stress (Figs. 4.20b and 4.20c).

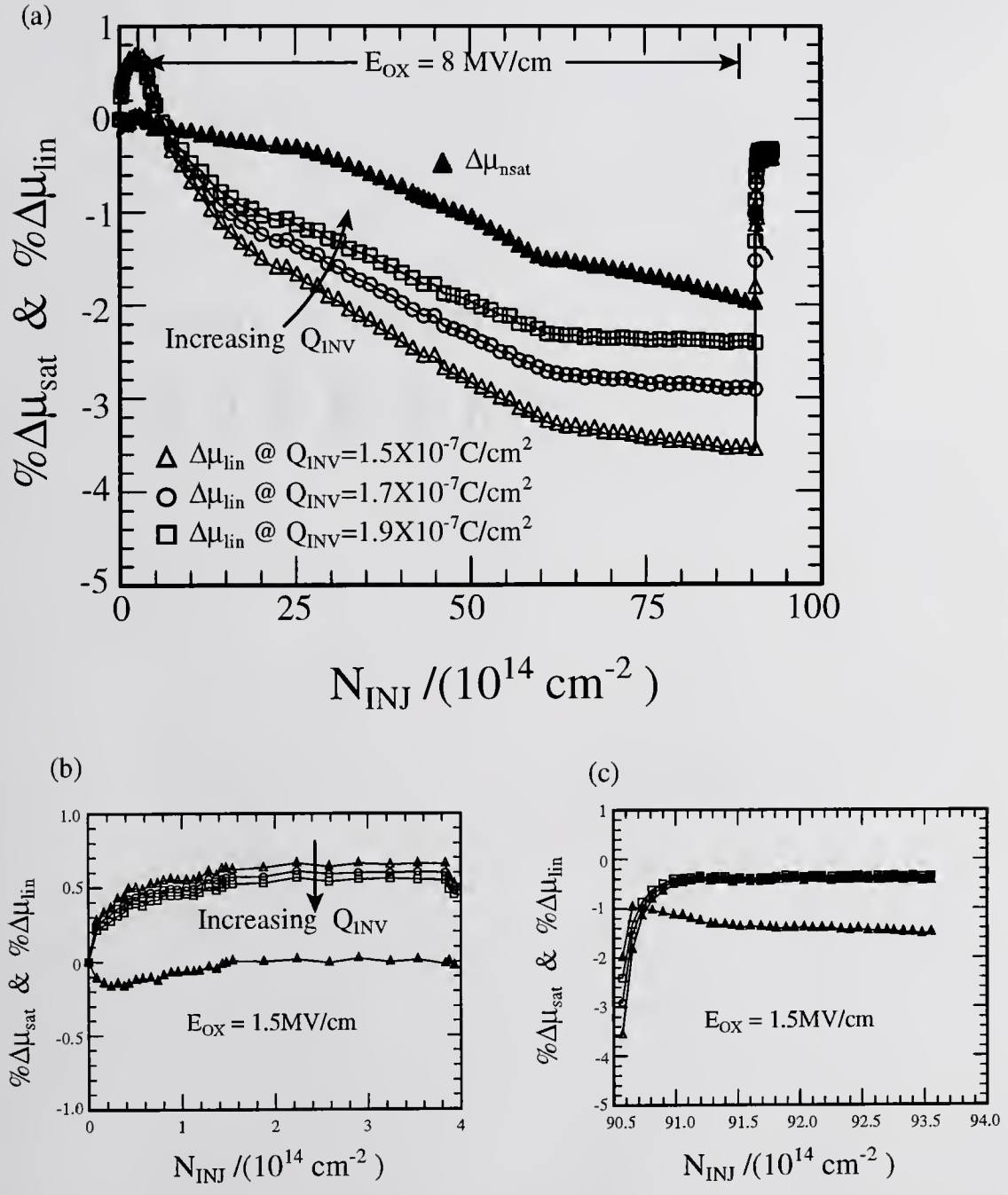



Figure 4.19 Percent degradation of the mobility of an n-channel BiMOST during SHEi at $E_{OX}$=1.5MV/cm enlarged in (b) for $N_{INJ} < 4 \times 10^{14}$, followed by FNTEi from the poly-gate at $E_{OX}$=8MV/cm, for $4 \times 10 < N_{INJ} < 9 \times 10^{15}$ and again by SHEi at $E_{OX}$=1.5MV/cm for $9 \times 10^{15} < N_{INJ} < 9 \times 10^{15}$ in (c). The value of $I_{D\text{-}sat}$ was extracted at a constant $V_{D\text{-}sat}=V_{G\text{-}sat}$ plus $\Delta V_{GT}$.

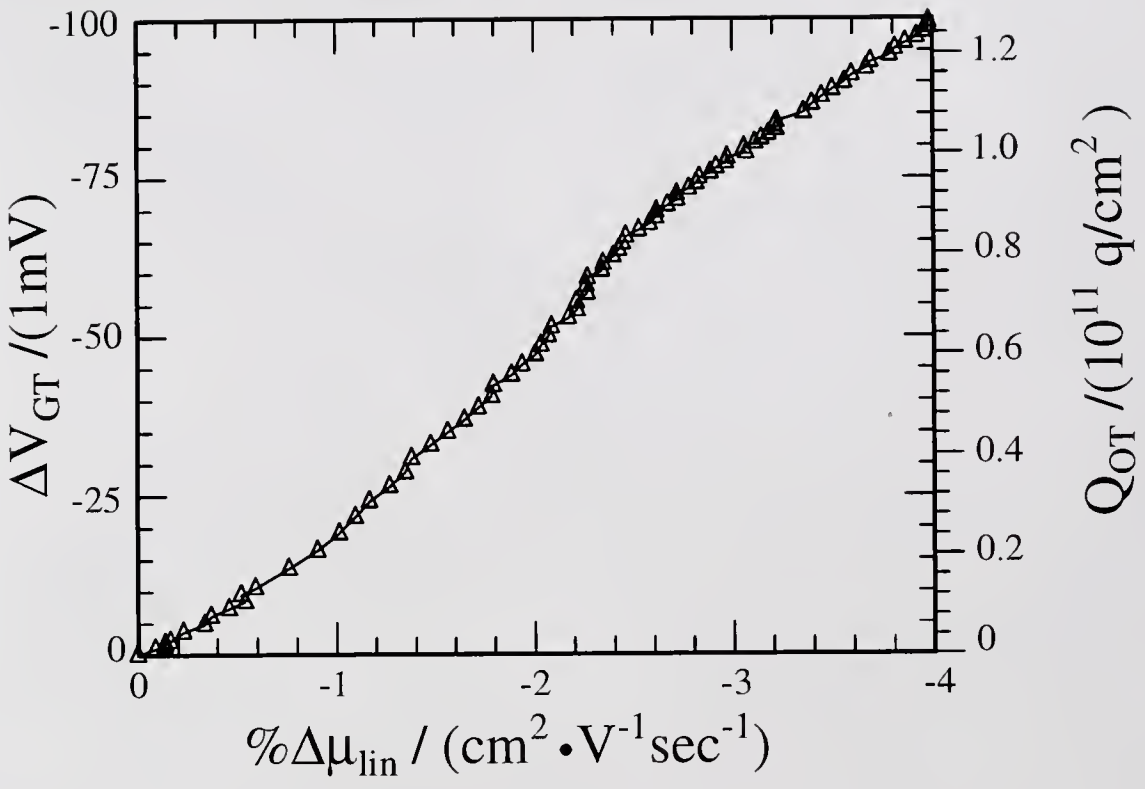



Figure 4.19 d Effective electron mobility shift versus the impact-emission generated $+Q_{OT}$, trapped in the gate oxide during the high-field FNTEi.

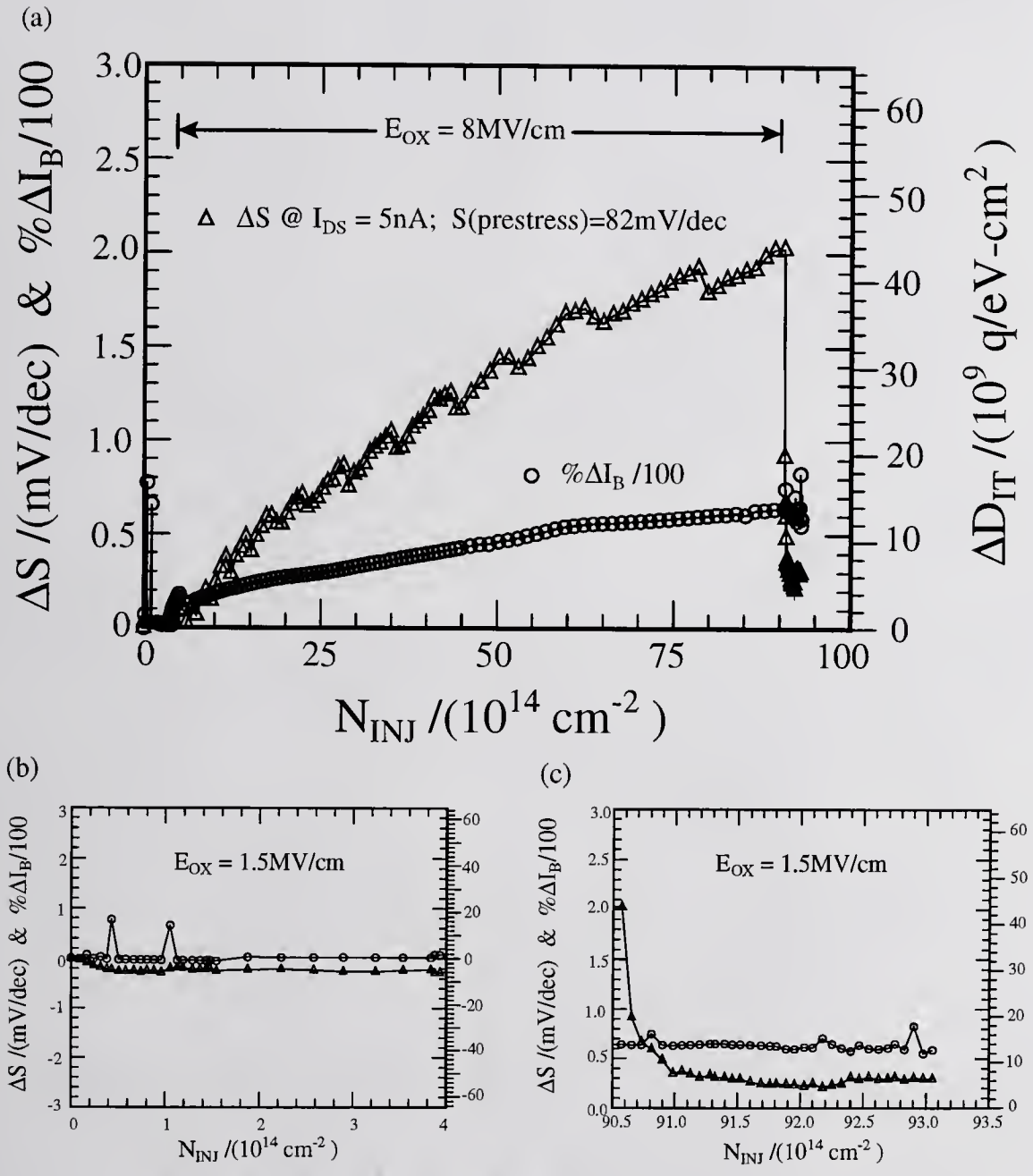



Figure 4.20 (a) Subtheshold slope and base current degradation of n-channel BiMOST during SHEi at $E_{OX}$= 1.5MV/cm enlarged in (b) for $N_{INJ} < 4 \times 10^{14}$, followed by FNTEi from the gate at $E_{OX}$ = 8MV/cm, for $4 \times 10^{14} < N_{INJ} < 9 \times 10^{15}$ ,and again by SHEi at $E_{OX}$=1.5MV/cm for $9 \times 10^{15} < N_{INJ} < 9.4 \times 10^{15}$ enlarged in (c).

However, some $D_{IT}$ are generated during the FNTEi portion of the stress. Interestingly though the subthreshold slope recovers to within 10% of its original value during the second SHEi stage whereas the shift in $I_B$ remains constant. This is most likely due to the fact that the subthreshold swing is sensitive to the areal nonuniformity of the oxide traps from charging and discharging in addition to the stress-generated interface traps, whereas the peak value of $I_B$ depends only on the change or increase of the recombination rate from the increasing density of the interface traps. Hence the fact that $\Delta S$ recovers and $\Delta I_B$ does not indicates that trap charging and discharging are nearly areally uniform in these experiments. And the experiments demonstrate again that $\Delta S$ is not as sensitive and unambiguous as $\Delta I_B$ in monitoring the interface traps.

## 4.3 Charging and discharging the shallow oxygen vacancy center at $E_C - 1eV$

Thompson [57] in his doctoral thesis also investigated the shallow level associated with the oxygen vacancy located at $E_C - 1eV$ below the oxide conduction band. Since electrons trapped at this level are easily thermally emitted or detrapped at room temperatures the 1eV level was filled at 77°K using low field SHEi stress. Then the electrons were tunneled out of the trap to the oxide conduction band using the isochronal electric field-stimulated emission (EFSE) technique. In this measurement the oxide electric field is incrementally increased by the applied gate bias with the source, drain, well, and substrate grounded for a predetermined amount of time. As $E_{OX}$ increases, the trap to band tunneling probability increases until the trapped electrons are emitted from the shallow traps. In this section the effects of charging and

discharging this shallow 1eV center on the mobility and saturation current will be illustrated.

In this SAM experiment, as in the previous ones, it is essential that the IV and CV characterization measurements are limited to a range of gate bias voltages lower than that applied during the stress in order that the trapped electrons are not field emitted from the shallow 1eV level during the measurement. This cannot be attained at room temperature because of rapid thermal emission of trapped electrons to the oxide conduction band from the shallow level. Therefore, in order to obtain an adequately long $V_G$ sweep for extracting $\mu_{lin}$ while keeping the oxide electric field sufficiently low (<1MV/cm), an n-channel BiMOST with a thick gate oxide was used with $X_{OX}$=290Å and a circular geometry of W/L=16.8. After immersing the packaged BiMOST into liquid nitrogen in the computer-controlled dewar, a 5MV/cm field is applied across the oxide for 5 minutes to ensure that all the shallow 1eV levels are empty. Next the BiMOST is biased for SHEi at a low gate oxide electric field of 1MV/cm. Since the injection efficiency is rather poor at such a low field the collector/base junction reverse bias was set to 7V and the emitter/base junction was biased at 3V initially.

Figure 4.21 plots the shift in the threshold voltage versus the injection/emission time, since the gate current is negligible during the emission portion of the stress and does not contribute significantly to $N_{INJ}$. The emission time for each $V_G$ increment of 0.3V was approximately 10 seconds. In Figure 4.22 the emission portion of the stress is plotted versus the increasing gate oxide field illustrating the $V_{GT}$ recovery as the trapped electrons are emitted. In Figures 4.23 and 4.24 the shift in $I_{D\text{-}sat}$ is plotted for

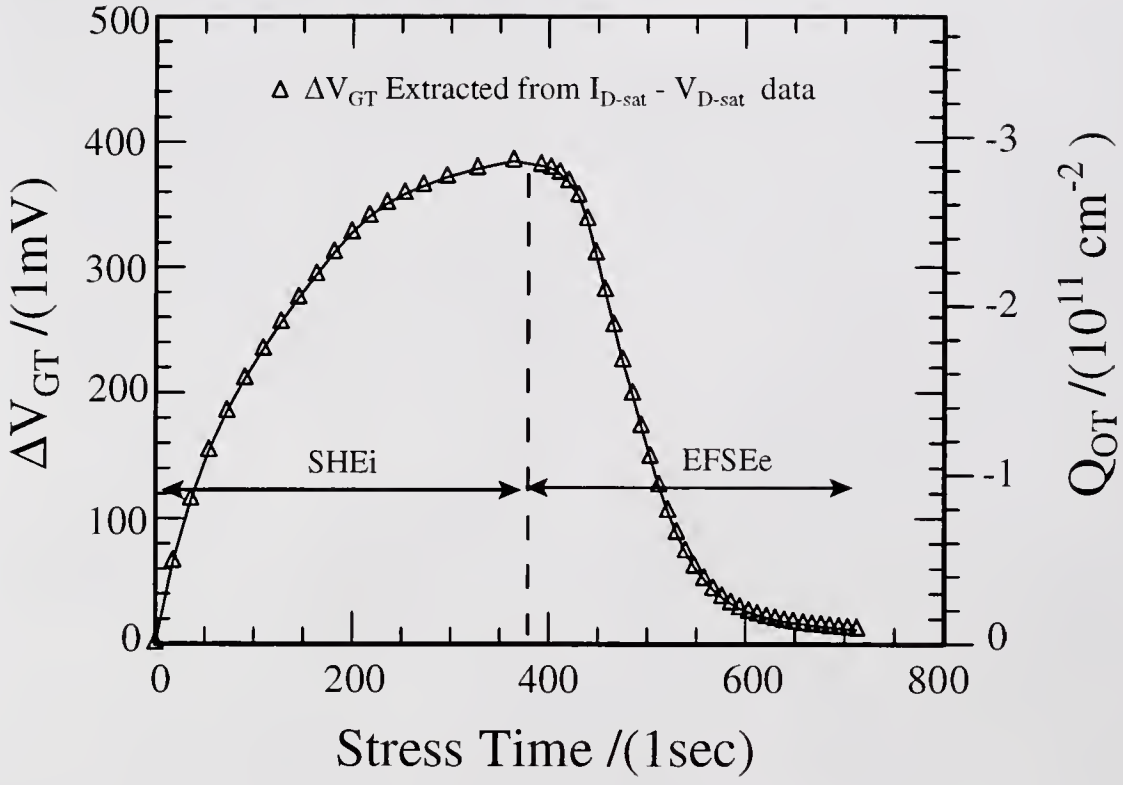



Figure 4.21 Threshold voltage shift of an n-channel BiMOST during SHEi stress at a constant $E_{OX}$=1MV/cm and $V_{CB}$=7V, followed by isochronal EFSE for t>400sec.

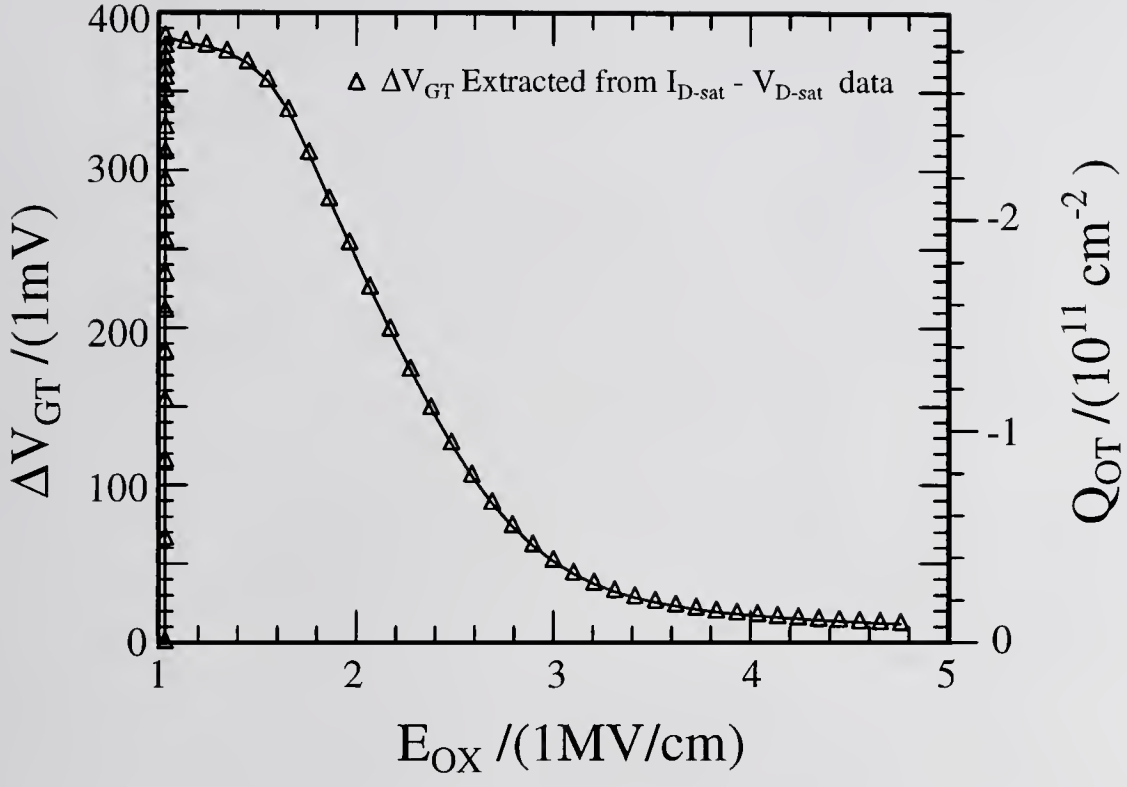



Figure 4.22 Threshold voltage shift of an n-channel BiMOST during isochronal EFSE versus the gate oxide electric field $E_{OX}$.

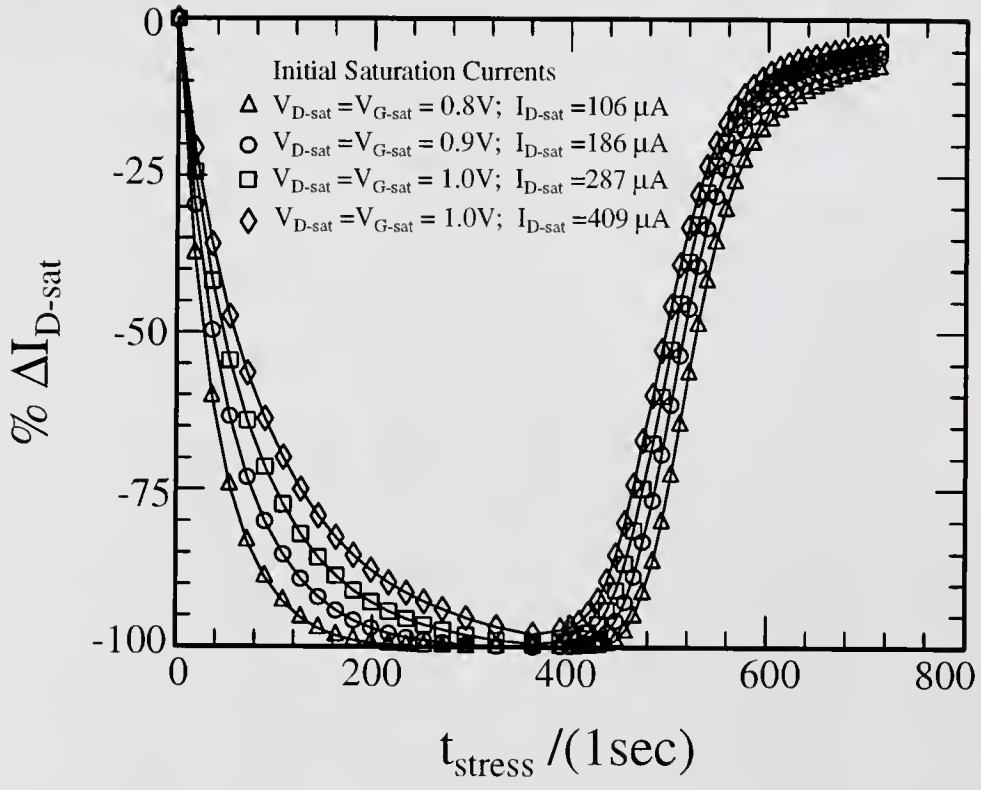



Figure 4.23 Shift in the saturation current of an n-channel BiMOST due to SHEi stress at a constant $E_{OX}$= 1MV/cm and $V_{CB}$=7V, followed by the isochronal EFSE for t>400sec. The value of $I_{D\text{-}sat}$ was extracted at a constant value of $V_{D\text{-}sat} = V_{G\text{-}sat}$.

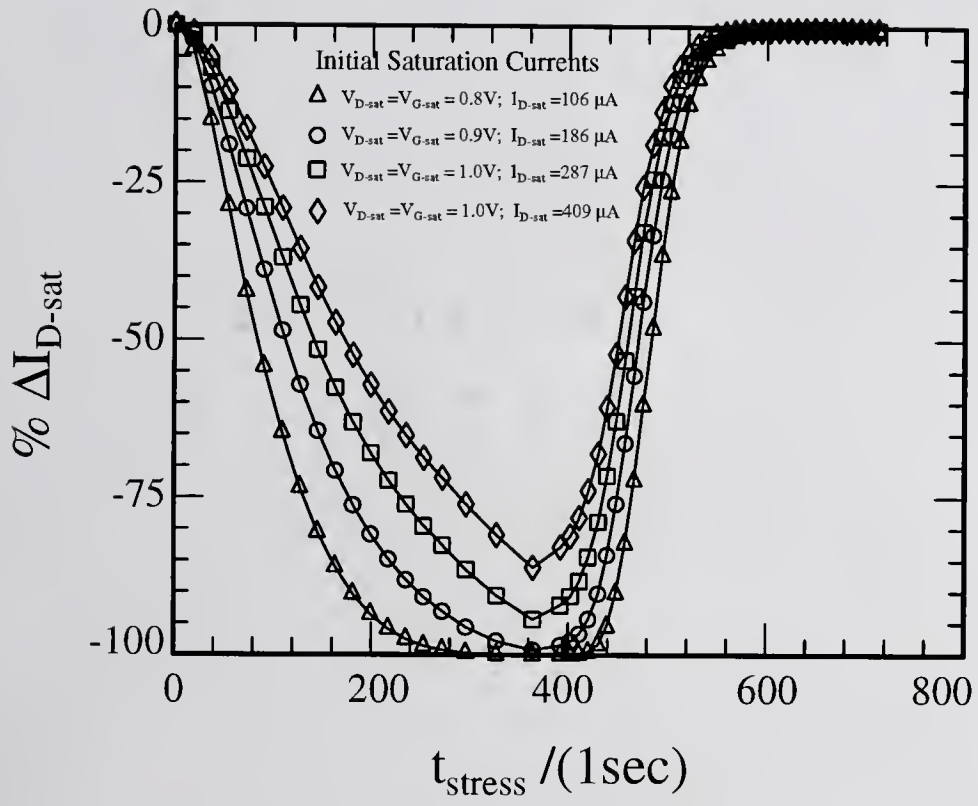



Figure 4.24 Shift in the saturation current of an n-channel BiMOST due to SHEi stress at a constant $E_{OX}$= 1MV/cm and $V_{CB}$=7V, followed by the isochronal EFSE for t>400sec. The value of $I_{D\text{-}sat}$ was extracted at a value of $V_{D\text{-}sat} = V_{G\text{-}sat}$ adjusted by $\Delta V_{GT}$.

the constant $V_D=V_G$ and the $V_D=V_G+\Delta V_{GT}$ cases as before. Though the value of $I_{D\text{-}sat}$ decreases largely due to the shift in $V_{GT}$ there appears to be a significantly larger decrease in $\mu_{sat}$ seen in the $V_{GT\text{-}adjusted}$ plot (Fig. 4.24). The degradation and recovery in $\mu_{lin}$ and $\mu_{sat}$ are shown in Figure 4.25 where $\mu_{lin}$ is plotted for three different values of constant $Q_{INV}$. The magnitude of $\Delta\mu_{lin}$ is significantly smaller than that of $\Delta\mu_{sat}$. This may be due to the fact that the $V_{D\text{-}sat}=V_{G\text{-}sat}$ values for extracting $I_{D\text{-}sat}$ remain constant during the stress even though there is a large shift in $V_{GT}$ as shown in Figure 4.21. This would cause a significant change of the voltage drop and longitudinal electric field in the drain junction space-charge region from the carrier depletion point in the channel to the drain junction, which would alter the buildup rate of the oxide charge and interface traps. Therefore, the range of current used in the two-parameter ($V_{GT}$, $\mu_{sat}$) least-squares-fit to the Sah-Pao model is changed after each stress. For example, a large positive $V_{GT}$ shift would have shifted the data closer to the subthreshold range where the Sah-Pao bulk-charge model does not apply. Nevertheless both mobilities decrease as expected with the increasing trapped electron charge in the oxide due to the corresponding increase in Coulombic scattering. The mobilities also recover as expected when the electrons are tunnel emitted out of the shallow traps leaving them in the neutral charge state and decreasing the Coulombic scattering. Plotting the degradation of the effective mobility during the initial low-field $-Q_{OT}$ charging stage versus the negative oxide charge density extracted from the $\Delta V_{GT}$, a linear dependence on $-Q_{OT}$ is observed as shown in Fig. 4.26. This is similar to that shown in Fig.4.19d for the $+Q_{OT}$ and provides a second experimental proof of electron mobility reduction

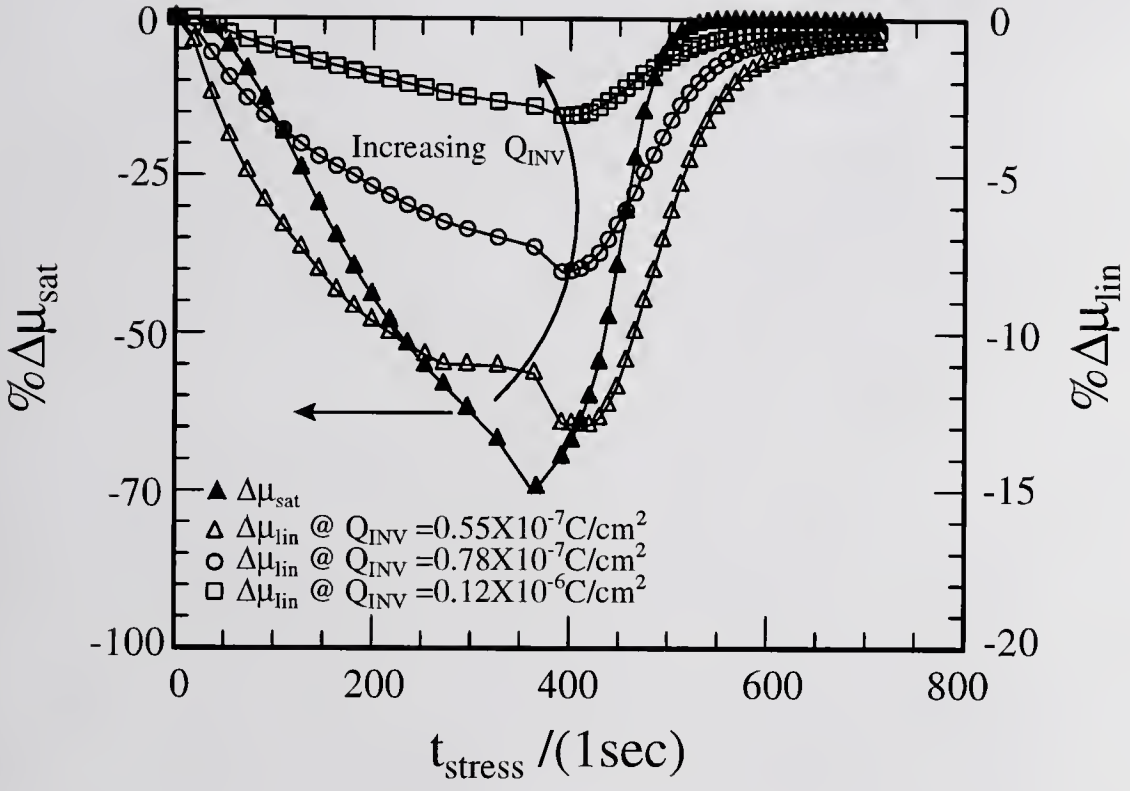



Figure 4.25 Percentage shift in the conductivity effective mobility, $\mu_{lin}$, for varying values of $Q_{INV}$, and in the saturation effective mobility, $\mu_{sat}$ plotted versus time for an n-channel BiMOST during SHEi stress at constant $E_{OX}$=1MV/cm and $V_{CB}$ = 7V, followed by the isochronal EFSE for t > 400sec.

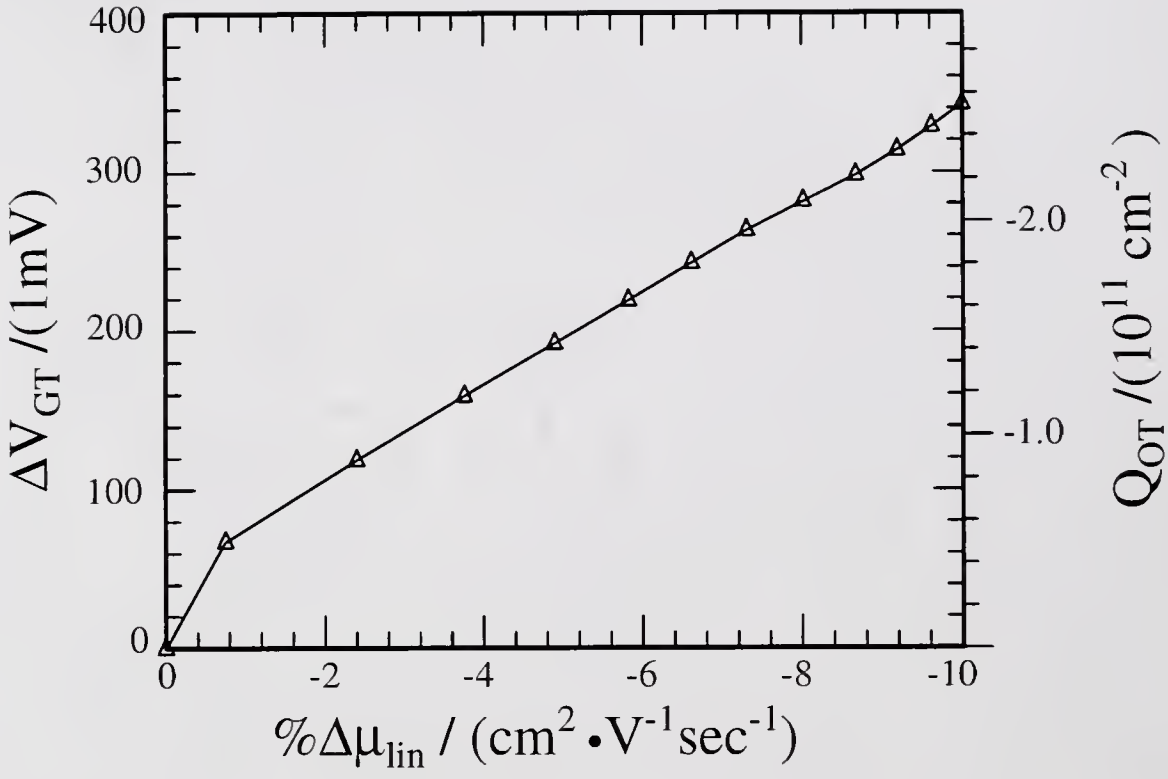



Figure 4.26 Shift of the effective conductivity electron mobility during the low-field SHEi filling of the shallow electron traps in the gate oxide versus the negative oxide charge density.

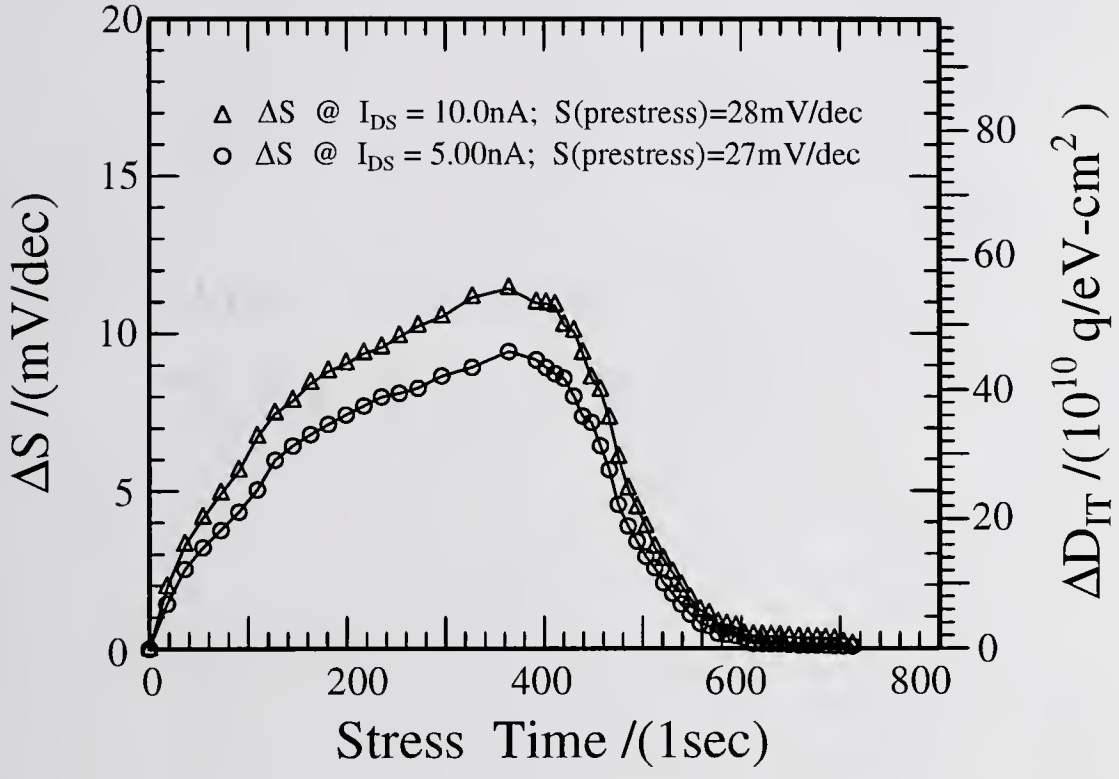



Figure 4.27 Shift in the subthreshold slope, S, of an n-channel BiMOST due to the build-up of interface states and/or nonuniform charging during SHEi stress at a constant $E_{OX}$=1MV/cm.and $V_{CB}$=7V, followed by isochronal EFSE for t > 400sec.

from Coulomb scattering of the channel electrons by positive and negative charge states of oxide traps at the same location in the oxide.

Finally the subthreshold swing and the corresponding calculated $D_{IT}$ are shown in Figure 4.27. The recovery shows that $\Delta S$ is most likely due to areal nonuniformity in the oxide charge as discussed previously rather than true interface state generation and annealing since such a large number ($10^{11}/cm^2$) of interface states would not be expected during low, 1MV/cm, SHEi stress, and in addition, there is not a viable physical mechanism to anneal out the interface states. This is collaborated with the $\Delta I_B$ change during the low field SHEi shown in Fig. 4.20 which shows no changes during the "annealing" cycle when $\Delta S$ reduces to zero while $\Delta I_B$ remains high.

This data will be expanded upon in the following chapter to illustrate the separation of interface states and areal charge nonuniformity.

# CHAPTER 5
# SEPARATION OF INTERFACE TRAPS AND AREAL OXIDE CHARGE NONUNIFORMITY

The interface-trap caused distortion of the gate capacitance-voltage ($C_g$-$V_G$ or CV) characteristics of the MOSC [10, Fig.403.1 on p.324] and the d.c. $I_D$-$V_G$ (IV) characteristics of the MOST in both the subthreshold and the inversion ranges [10, section 628 on pp.653-662] are well documented in the literature. However it is also well-known that an areally nonuniform distribution of charged oxide traps ($Q_{OT}$) will distort the CV and IV characteristics. In addition, the IV characteristic is also distorted by the channel mobility variation with $V_G$ as discussed in chapter 2 and illustrated in chapter 4. In the last chapter it was shown that the MOST subthreshold swing, $\Delta S$, and base current change, $\Delta I_B$, could be used to monitor the increase in interface traps but that they could also be affected by areally (y-direction) nonuniform trapped oxide charge. In this chapter a rapid and highly sensitive electrical measurement technique is proposed and demonstrated [59] which is designed to separate the effects on the CV and IV characteristics from stress-induced areal nonuniform interface and oxide traps.

This new technique combines the DCIV and $\Delta S$ methods to analyze samples stressed by uniform and nonuniform SHEi, SHEi+CHEi, and FNTEi to uniformly and nonuniformly charge and discharge the oxide traps via impact emission, low field thermal capture, and EFSE emission transitions discussed in chapter 4. For example, it

was suggested that the constant $I_B$ (unchanged during the low field SHEi stress) and the changing distortion of the subthreshold swing in Figure 4.20c implied the presence of areally inhomogeneous oxide charge generated during the 8MV/cm FNTEi stress (Fig.4.20a). The design of experiments in this chapter is based solely on the assumption that interface traps generated during the high field (FNTEi or SHEi/CHE) or low field (SHEi) phase-1 will not be removed or annihilated during the EFSE emission or the low field SHEi neutralization of $Q_{OT}$ during phase-2. Therefore any stress-generated $\Delta I_B$ increase, due to $\Delta D_{IT}$, during phase-1 will be preserved during phase-2, while the stress-generated areally nonuniform $\Delta Q_{OT}$ in phase-1 will be neutralized during phase-2. The results presented in this chapter demonstrate: 1) the separation of the generated interface traps, $\Delta D_{IT}$, from the areally nonuniform charging and uniform neutralization of the oxide traps, $\Delta Q_{OT}$, 2) that charging $+Q_{OT}$ by high field SHEi with $V_{DS}$=0 is areally uniform whereas 3) charging $+Q_{OT}$ by FNTEi is areally nonuniform, and 4) that low field (<1MV/cm) $-Q_{OT}$ charging at 77°K is also areally nonuniform.

## 5.1 Nonuniform $+Q_{OT}$ via FNTEi

One possible explanation to describe the nonuniformity of the FNTEi in MOST's is that the oxide voltage drop ($V_{OX}$) in the gate/source and gate/drain overlap regions differs from that in the channel or well region because of the difference in doping impurity concentrations, n+ in the source and drain, and p or p- in the channel or well. It is pointed out (chapter 3 of [10,54]) that the difference between the gate bias

($V_G$) and the oxide voltage drop ($V_{OX}$) is due to three factors: 1) the total potential drop in the polysilicon gate, $V_{S\text{-}gate}$, and silicon substrate, $V_{S\text{-}subs}$, 2) the gate/substrate work function difference, $\Phi_{GX}$, and 3) the charged oxide and interface traps:

$$V_{OX} = V_G + V_{S\text{-}gate} + V_{S\text{-}subs} + \Phi_{GX}$$
$$= V_G + V_{S\text{-}gate} + V_{S\text{-}subs} + V_{FB} \qquad 5.1$$

where $\Phi_{GX}$ is equal to the flatband voltage ($V_{FB}$) if $Q_{OT}$ and $Q_{IT}$ are negligible ('X' denotes the silicon substrate, G the gate, and S the gate/oxide and oxide/substrate interface position). For example, $V_{FB}$ for a sample with an $n^+$-poly-gate concentration of $N_{GG} = 1x10^{20}$ phosphorus/cm$^3$ and a p-well concentration of $P_{XX} = 3\times10^{16}$ boron/cm$^3$ is $V_{FB} \equiv V_{F\text{-}gate} - V_{F\text{-}channel} \simeq -(k_bT/q)\log_e(N_{GG}P_{XX}/n_i^2) \simeq -0.93V$ whereas $V_{FB}$ in the gate overlap regions of the self-aligned $n^+$ source/drain is $V_{FB} = -(k_BT/q)\log_e(N_{GG}/N_{DD}) \simeq 0V$. In addition to the difference in $V_{FB}$, the silicon surface energy band bending in the p-well, $V_{S\text{-}well}$ or $V_{S\text{-}channel}$, will be greater than that in the $n^+$source/drain regions, $V_{S\text{-}source}$ and $V_{S\text{-}drain}$ because of the lower dopant impurity concentration in the well and channel and higher dopant impurity concentration in the drain and source, in addition to their opposite conductivity type. The total potential drop in the silicon gate and substrate, $V_{S\text{-}gate}$, $V_{S\text{-}channel}$, $V_{S\text{-}drain}$ and $V_{S\text{-}source}$, has two contributions: 1) the potential drop in the accumulation or inversion layer ($V_{S\text{-}acc}$ or $V_{S\text{-}inv}$) and 2) the potential drop in the surface space charge layer when biased into inversion. The second component is zero in accumulation and twice the bulk potential ($2V_F$) in inversion. Hence, given a particular gate bias condition, $V_G$, and neglecting any potential drop in the highly doped polysilicon gate, the oxide voltage drop in the region over the p-well and the source/drain overlap regions is

$$V_{OX\text{-well}} = V_G - V_{FB} - V_{S\text{-well}} \quad 5.2$$

$$V_{OX\text{-source/drain}} = V_G - V_{FB} - V_{S\text{-source/drain}} \simeq V_G \quad 5.3$$

Therefore during the accumulation stress of an n-BiMOST by FNTEi from the poly-gate ($V_G$ = -13.6V), the voltage drop in the oxide, $V_{OX}$, will be higher at the edge of the channel and in the source and drain overlap regions than in the the channel over the p-well since $|V_{FB}| >> |V_{S\text{-well}}|$ or $|V_{OX}| \simeq |V_G| - |V_{FB}|$. The higher $V_{OX}$ in the source/drain regions would then give rise to significantly higher Fowler-Nordheim tunneling injection current passing through the edge and source-drain regions of the oxide due to the exponential dependence of $I_G$ on $E_{OX}=V_{OX}/X_O$. Furthermore, the higher $V_{OX}$ near the source and drain will result in increased $+Q_{OT}$ generation in these regions since more carriers will gain the required kinetic energy (>7eV) to impact emit the trapped electrons at the oxygen vacancy sites. The results of this case were presented in Figures 4.16-4.20. Figure 4.20c (phase-2) illustrated the recovery in $\Delta S$ but not $\%\Delta I_B$ during the low field SHEi which neutralized the nonuniform $+Q_{OT}$.

Conversely, under the inversion stress ($V_G > 0$ in nMOST) the surface in the p-well region is inverted, and electrons in the silicon substrate will tunnel through the gate oxide layer into the poly-Si gate. The negative flatband voltage over the p-well would increase $V_{OX}$ by approximately 0.93V in the center of the channel over the p-well compared to the source and drain edge regions. However, the flatband voltage is now compensated by the potential drop in the p-silicon well or substrate to invert the surface to n-type and create the n-channel. This potential drop is $V_{S\text{-channel-inv}} = 2V_{F\text{-well}}$ so the total voltage difference between $V_G$ and $V_{OX}$ is rather small, $2V_{F\text{-channel}} + V_{S\text{-channel-inv}} \geq \simeq 0$.

Thus, a FNTEi/SHEi stress-and-measure or SAM experiment was conducted with positive $V_G$ applied polarity to the poly-gate (inversion) in order to tunnel electrons from the silicon substrate into the oxide and to impact emit the trapped electrons at the neutral nonbridging oxygen vacancy centers in order to buildup positive oxide charge. The source, drain, well and emitter of the BiMOST were all grounded with respect to the gate electrode which was set to $V_G$ = +13.6V to determine if the areally nonuniform positive oxide charge distribution could be produced during the inversion FNTEi stress of this nBiMOSTs. Figure 5.1a illustrates the negative gate voltage shift, $\Delta V_G$, during the high field FNTEi portion of the stress and the subsequent recovery (Fig. 5.1b) during the low field thermal electron capture (SHEi) to neutralize the $+Q_{OT}$. Figure 5.1c illustrates the corresponding increase of the subthreshold swing, $\Delta S$, (measured at $I_D$=5nA and $V_{DS}$=100mV) and the percent shift in the peak base current, $\%\Delta I_B$ (measured at $V_{BE}$=0.5V) during phase-1. Figure 5.1d illustrates a recovery, by ~60%, in $\Delta S$ towards its original value while the $\%\Delta I_B$ due to $\Delta D_{IT}$ remains constant during the phase-2 low field SHEi which neutralized the $+Q_{OT}$. This is essentially the same result obtained under accumulation FNTEi stress discussed in the previous chapter (Figs. 4.16 and 4.20). The recovery of $\Delta S$ indicates that an areally nonuniform distribution of positive oxide charge was generated during the high field FNTEi which was then neutralized during the low field SHEi. The corresponding increase in $I_B$ during the high field FNTEi without the subsequent recovery during the low-field SHEi is an indication of the expected $+Q_{IT}$ generated by high-field FNTEi stress. These results are consistent with the theory and demonstrate the separation of $Q_{IT}$ and the areally nonuniform $+Q_{OT}$.

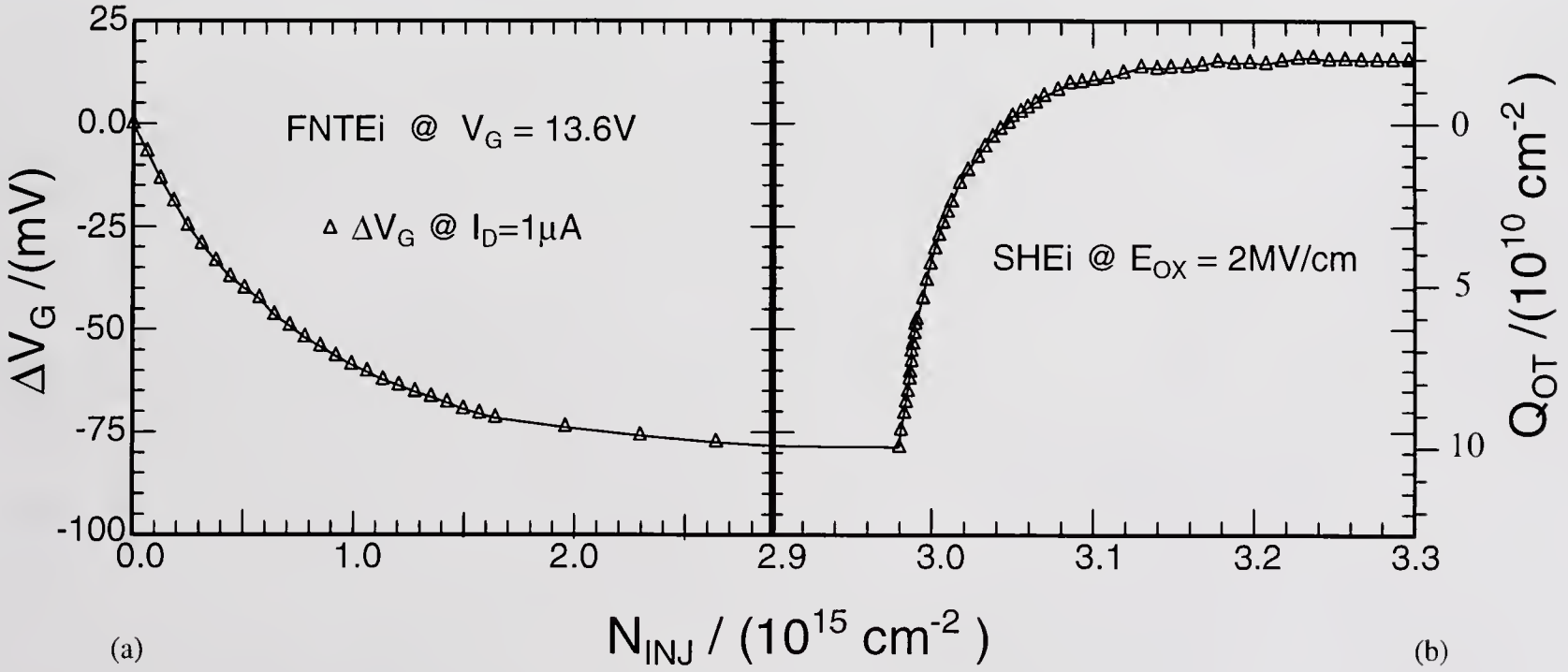



Fig. 5.1 (a) Change in threshold gate voltage, $\Delta V_G$, during areally nonuniform positive charging by FNTEi (phase-1) stress at $V_G$=13.6V.
(b) Change in threshold gate voltage, $\Delta V_G$, during areally uniform $+Q_{OT}$ neutralization by low field SHEi (phase-2) stress at $V_G$=3.4V and $V_{DS}$=0V.

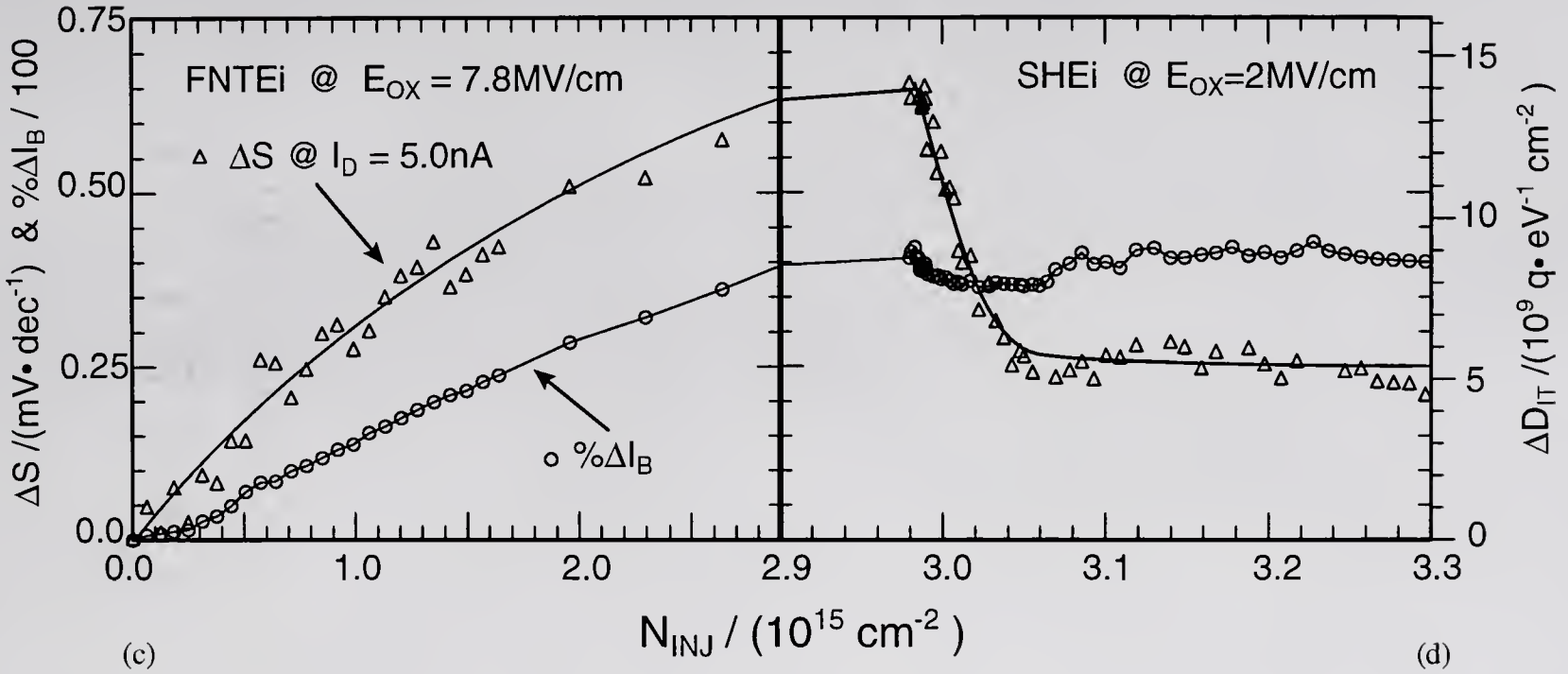



Fig. 5.1 (c) Change in subthreshold swing, $\Delta S$, and base current, $\Delta I_B$, during areally nonuniform positive charging by FNTEi (phase-1) stress at $V_G$=13.6V.
(d) Change in subthreshold swing, $\Delta S$, and base current, $\Delta I_B$, during areally uniform $+Q_{OT}$ neutralization by low field SHEi (phase-2) stress at $V_G$=3.4V and $V_{DS}$=0V.

## 5.2 Room Temperature SHEi Stress

Positive charge can also be generated by SHEi using the BiMOST structure [56] to give both areally uniform and nonuniform distributions of $+Q_{OT}$ as long as $V_{OX}$ exceeds the 7V threshold. The uniformity of the SHEi can be controlled by the d.c. voltage applied between the source and the drain ($V_{DS}$) which alters the gate oxide electric field, $E_{OX}$, in the y-direction along the channel. Thus two SAM experiments were performed, one with $V_{DS}$=0V during the phase-1 SHEi to verify the assumed areal uniformity of $Q_{OT}$ and $D_{IT}$, and the other with $V_{DS}$=4V during phase-1 SHEi to generate the nonuniform $Q_{OT}$ and $D_{IT}$. The results provide further support for the methodology of separating $D_{IT}$ from areally nonuniform $+Q_{OT}$.

### 5.2.1 Uniform Oxide and Interface Traps

The first experiment employs the assumed (and confirmed by the results) uniform SHEi stress, due to setting $V_{DS}$=0V. During phase-1, the high-field ($E_{OX}$=7.3MV/cm; $V_G$=12.8V) SHEi stress, $+Q_{OT}$ are generated in the oxide as confirmed by the negative $\Delta V_{GT}$ (Fig. 5.2a) via the same impact emission process at the oxygen vacancy center discussed previously. This is then followed by the low-field (2MV/cm) SHEi neutralization ($\Delta V_G$ recovers) of the $+Q_{OT}$ (Fig. 5.2b). Both $\Delta S$ and $\Delta I_B$ increased during phase-1 and were roughly proportional to each other as expected. Figure 5.2d shows that both $\Delta S$ and $\Delta I_B$ remained constant during phase-2 indicating

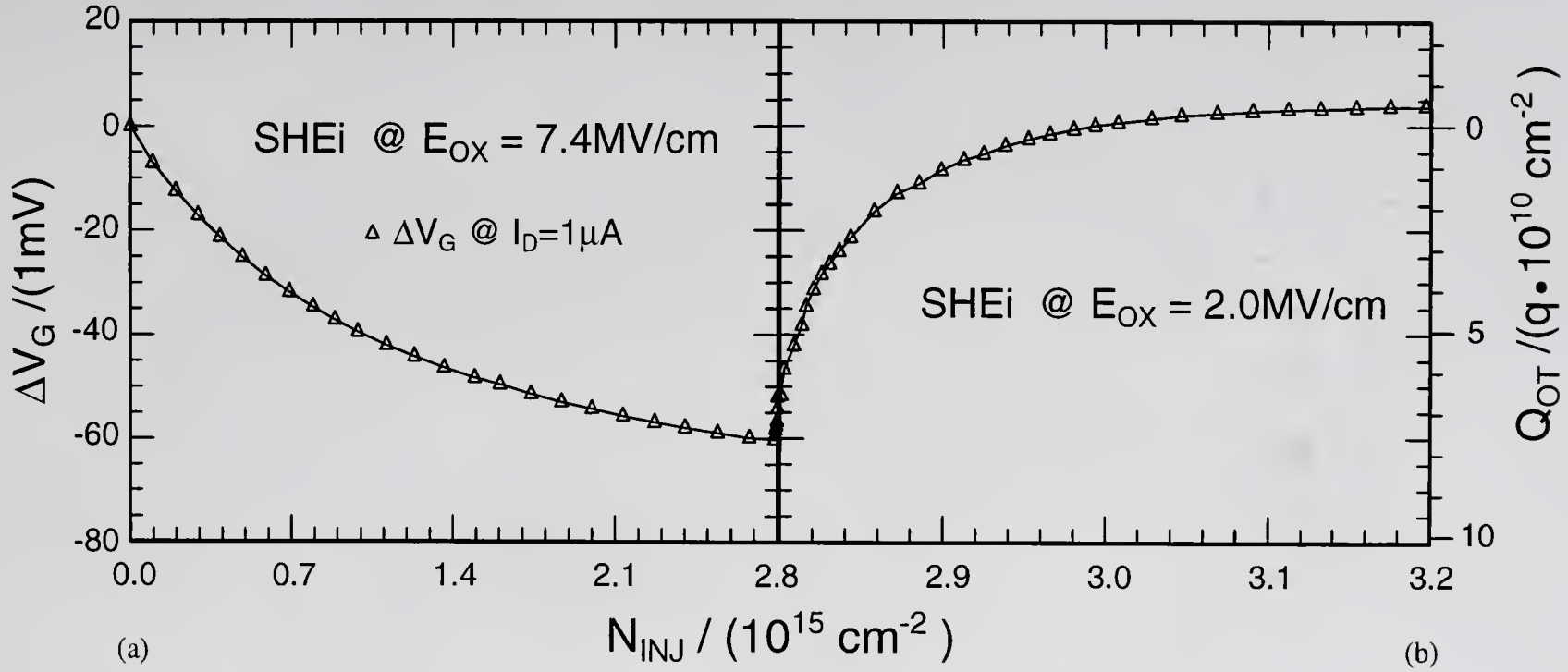



Fig. 5.2 (a) Change in threshold gate voltage, $\Delta V_G$, during areally uniform positive charging by high field SHEi (phase-1) stress at $V_G$=12.8V and $V_{DS}$=0V.
(b) Change in threshold gate voltage, $\Delta V_G$, during areally uniform $+Q_{OT}$ neutralization by low field SHEi (phase-2) stress at $V_G$=3.4V and $V_{DS}$=0V.

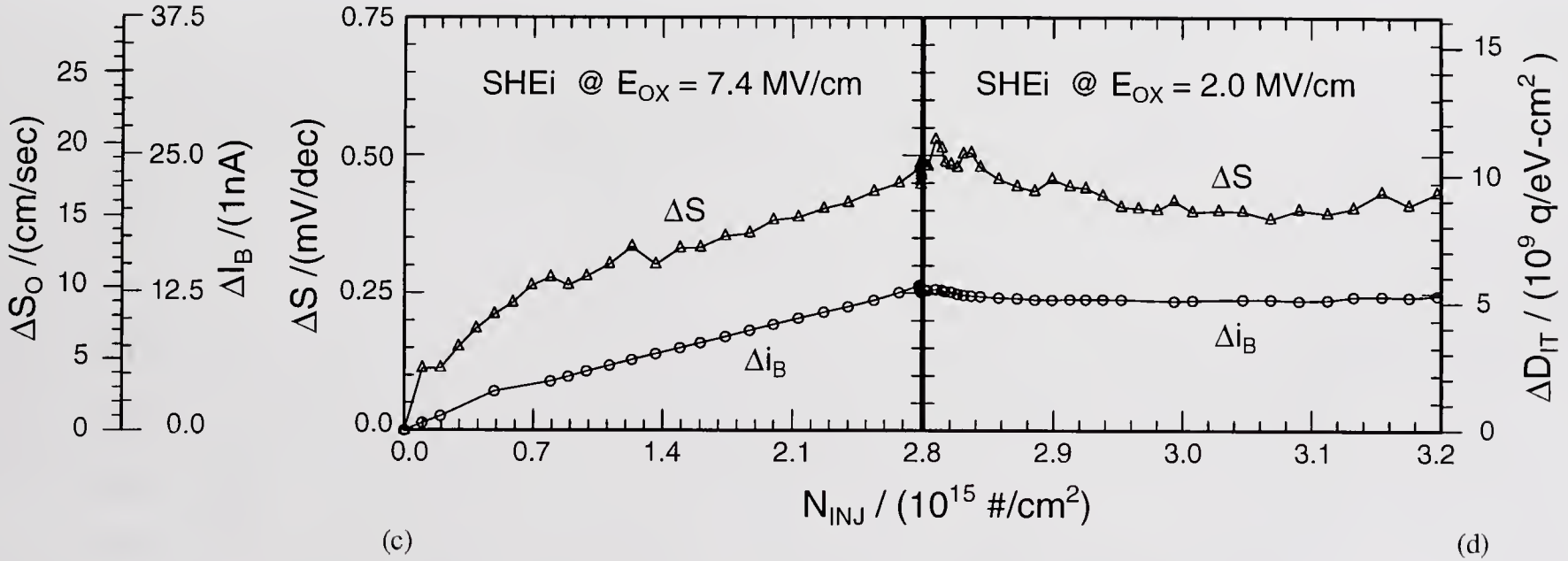



Fig. 5.2 (c) Change in subthreshold swing, $\Delta S$, and base current, $\Delta I_B$, during areally uniform positive charging by SHEi (phase-1) stress at $V_G$=12.8V and $V_{DS}$=0V.
(d) Change in subthreshold swing,$\Delta S$, and base current, $\Delta I_B$, during areally uniform $+Q_{OT}$ neutralization by low field SHEi (phase-2) stress at $V_G$=3.4V and $V_{DS}$=0V.

that $\Delta S$ must all be due to $\Delta D_{IT}$ and not areally nonuniform $+Q_{OT}$. Note also that $\Delta I_B$ was plotted instead of $\%\Delta I_B$ in order to illustrate the conversion to surface recombination velocity change, $\Delta S_O$. The ratio $\Delta S/\Delta I_B \simeq (0.50mV/decade)/12.5nA = 40k\Omega/decade$ and $\Delta D_{IT}/\Delta I_B = 10^{10}(states/eV\text{-}cm^2)/12.5nA = 8x10^8(states/eV\text{-}cm^2)/nA$ also illustrates the extremely high sensitivity of the new measurement technique for detecting interface traps. The change in the surface recombination velocity was calculated using (4.4) and $V_{BE}$=0.5V. Assuming equal carrier capture cross-sections $\sigma_n=\sigma_p=\sigma_0$ for electrons and holes at the interface trap, the recombination cross-section is given by (4.5) which is repeated here

$$\sigma_0 \simeq (2/\pi)\Delta S_0/(\Theta_{th}\,\Delta N_{IT}) \tag{5.4}$$

For an interface trap energy distribution width of 0.025eV (about one $k_BT$) and $\Theta_{th}\simeq 10^7 cm/s$

$$\sigma_0 \simeq (2/\pi)\Delta S_o/(\Theta_{th} \bullet \Delta D_{IT} \bullet k_BT)$$

$$\simeq (2/\pi)(10cm/s)(10^7 \bullet 10^{10} \bullet 0.025) \simeq 25\text{Å}^2 = \pi r^2 \simeq \pi(3\text{Å})^2 \tag{5.5}$$

or a radius of ~3Å which is consistent with the bond length of a localized dangling silicon bond.

### 5.2.2 Nonuniform Oxide and Interface Traps

To complement the areally uniform $+Q_{OT}$ results of the above experiment a second SAM experiment was run in which areal nonuniformity in $Q_{OT}$ and $Q_{IT}$ was generated during phase-1 using the SHEi and CHE stress. This was accomplished by applying a voltage between the source and drain, $V_{DS}=V_D-V_S>0$ which causes the

oxide voltage drop to vary from its highest value at the source, $V_{OS}=V_G-V_{GTS}-V_S$, to its lowest value at the drain, $V_{OD}=V_G-V_{GTD}-V_D$. The $V_{GTS}$ and $V_{GTD}$ are the gate threshold voltages at the source and drain ends of the channel respectively. Thus, if $V_G-V_{GTD}-V_D$ or the oxide voltage drop is less than the threshold voltage (~7V) for electron-impact emission at the $V_O$ center, then, $+Q_{OT}$ could not be generated in a length of the channel next to the drain. Then $+Q_{OT}=0$ in the length of the channel from the drain, $y=y_D$, to $y=y_7$, where $V_O(y_7)=7V$, and $+Q_{OT}$ will increase from $Q_{OT}(y_7)=0$ to $+\Delta Q_{OT}(y=0)$ at the source (y-direction along the length of the channel). A sensitive and reliable d.c. measurement of $Q_{OT}$ and $N_{IT}$ profiling (i.e. their y-position or channel-position dependence) will be reported [60]. A highly peaked $\Delta D_{IT}$ or $\Delta Q_{IT}$ at the drain junction is not expected here because $V_{DS}<V_{GS}$ so that the channel was not depleted and there was no high-field depleted space-charge region near the drain junction. Thus, the channel electrons were essentially at thermal equilibrium in this long channel. Hot electrons with high kinetic energies would be expected in shorter channels when the longitudinal electric field over a major part of the channel length is substantially larger than the critical electric field for hot electrons. Using the linear mobility obtained in Fig.4.3a, the critical field can be estimated from $E_{crit} \simeq \Theta_{sat}/\mu_{lin} = 10^7(V/cm)/500(cm^2/V\text{-}s) = 20kV/cm = 2V/\mu m$ [10, pp.668-669 and Fig.314.1 on p.252]. Nevertheless, even for long channels at low longitudinal electric fields, a somewhat nonuniform distribution of $\Delta Q_{IT}$ could be expected from the kinetic energy spread of hot holes which are back-injected from the polysilicon-gate into the oxide as recently demonstrated by Lu and Sah [61]. These oxide holes can drift to the oxide/silicon interface and break the weak interfacial hydrogen and silicon-oxygen

bonds to create a nonuniform distribution of interface traps. The voltage conditions were $V_G$=13.6V, $V_D$=4.0V, $V_S$=0V (grounded), $V_B$ = −4V and $V_{BE}$ = 0.55V. The $\Delta V_{GT}$, $\Delta I_B$ and $\Delta S$ results are shown in Figures 5.3a-5.3d. As in the previous experiments $|\Delta V_{GT}| >> \Delta S \approx 0.5$mV so that $\Delta V_{GT}$ is again mainly due to $+\Delta Q_{OT}$, but $\Delta S$ should also have a nonuniformity component (as in the FNTEi case, Figs. 5.1c and 5.1d) due to the nonuniform $+\Delta Q_{OT}$ and possibly nonuniform $\Delta Q_{IT}$ which will now be confirmed.

The $\Delta V_{GT}$ data (Figs. 5.3a and 5.3b) were obtained in strong inversion at $I_D$=1μA (filled circles and triangles) and 10μA (open circles and triangles). The data labeled 'Reverse' in this experiment were measured with the drain and source interchanged to monitor the damage (i.e. interface traps) near the drain junction since the subthreshold $I_D$-$V_G$ characteristics are sensitive to the interface traps located near the injecting junction (the source when $V_D$=0.1V or the drain when $V_S$=0.1V). During phase-1 the near coincidence of the forward and reverse $\Delta V_{GT}$ in strong inversion (10μA) and the 30% difference, $\Delta V_{GT\text{-reverse}}/\Delta V_{GT\text{-forward}} \approx (-43\text{mV})/(-33\text{mV}) \approx 1.3$, at a weaker inversion (1μA) indicate that the nonuniform $\Delta Q_{OT}$ and $\Delta Q_{IT}$ are screened out by the high electron density in the inversion channel. This is consistent with the results of Figs. 4.19a and 4.25 which show that the mobility is less influenced by $Q_{OT}$ at higher values of inversion charge density $N_{INV}$. The $+Q_{OT}$ charge buildup ($-\Delta V_{GT}$ shift) during phase-1, (Fig. 5.3a) is completely neutralized during phase-2 as $V_{GT}$ recovers (Fig. 5.3b).

The $\Delta I_B$ and $\Delta S$ measured in the subthreshold range are shown in figures 5.3c (phase-1) and 5.3d (phase-2). The results are similar to those of the uniform stress in

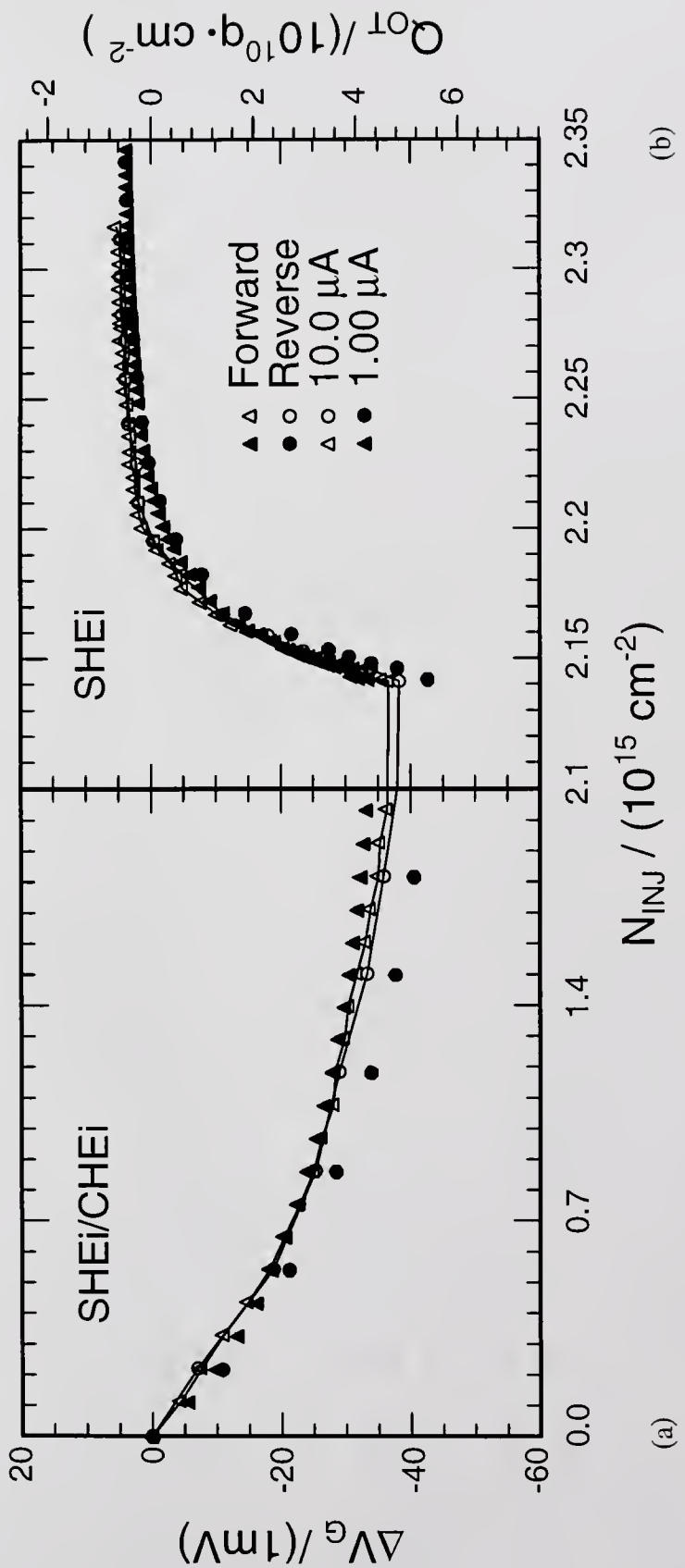



Fig. 5.3 (a) Change in threshold gate voltage, $\Delta V_G$, during areally nonuniform positive charging by high field SHEi/CHEi (phase-1) stress at $V_G$=12.8V and $V_{DS}$=4V.
(b) Change in threshold gate voltage, $\Delta V_G$, during areally uniform $+Q_{OT}$ neutralization by low field SHEi (phase-2) stress at $V_G$=3.4V and $V_{DS}$=0V.

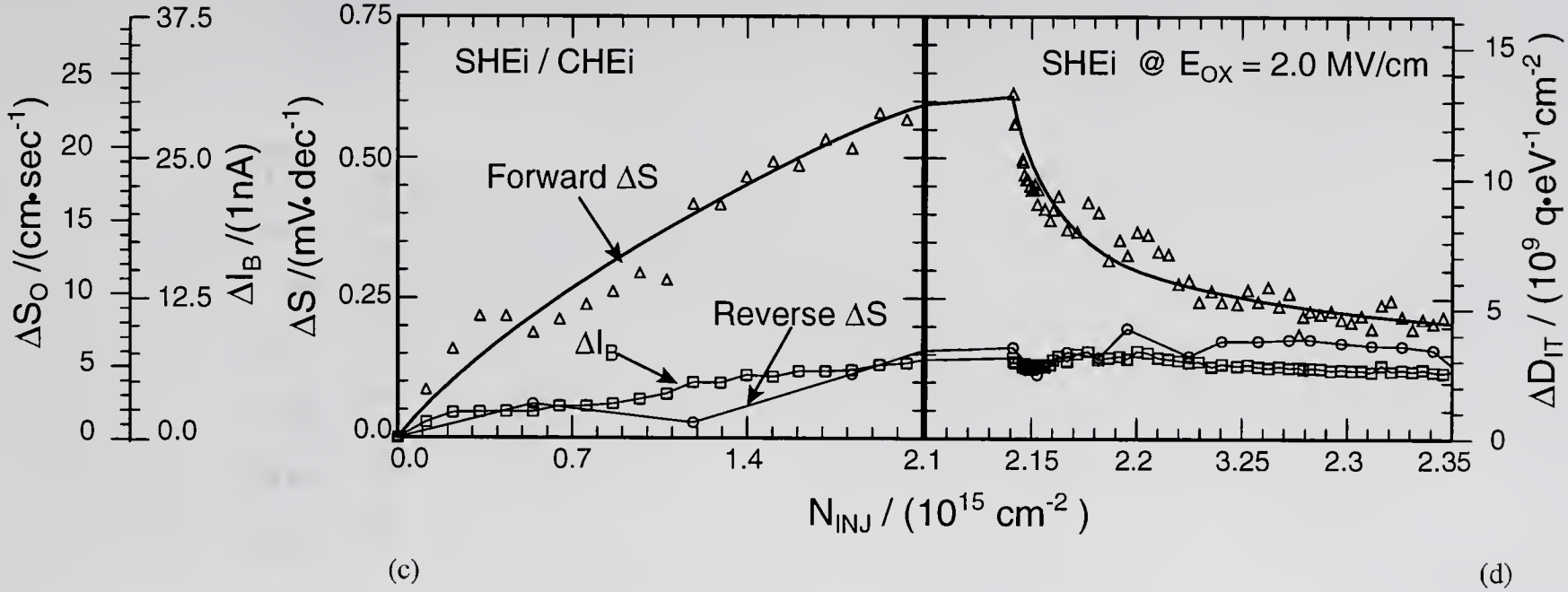



Fig. 5.3 (c) Change in subthreshold swing, ΔS, and base current, $\Delta I_B$, during areally nonuniform positive charging by SHEi/CHEi (phase-1) stress at $V_G$=12.8V and $V_{DS}$=4V.
(d) Change in subthreshold swing,ΔS, and base current, $\Delta I_B$, during areally uniform $+Q_{OT}$ neutralization by low field SHEi (phase-2) stress at $V_G$=3.4V and $V_{DS}$=0V.

figures 5.2c and 5.2d except that the nonuniform $\Delta Q_{OT}$ gives a large source-drain difference, $\Delta S_{source} \simeq 4\Delta S_{drain}$. Figure 5.3d shows that $\Delta S_{source}$ recovers during phase-2 from its maximum after phase-1 by $\simeq 0.63 - 0.23 \simeq 0.4$mV/decade due to neutralization of the nonuniform $+Q_{OT}$ while the remaining $\Delta S_{IT} = 0.23$mV/decade from $\Delta D_{IT}$ does not. This is confirmed by the fact that the ratio $\Delta D_{IT}/\Delta I_B = 5x10^9$(states/eV-cm$^2$)/6.25nA$=8x10^8$(states/eV-cm$^2$)/nA remained the same as in the uniform SHEi stress case calculated from figure 5.2d.

## 5.3 Low Temperature SHEi Results

In the last chapter it was also shown that significant areal nonuniformity was obtained when using low-field SHEi (1MV/cm) to charge the shallow $E_C-1$eV electron traps in the oxide at 77°K. Since high field SHEi at room temperature was shown to give uniform positive charge generation in section 5.2 the low-temperature low-field SHEi experiment was repeated while measuring the top-emitter base current [12] to monitor any increase in $\Delta D_{IT}$. The top-emitter $I_B$ measurement makes use of the source or the drain as the emitter for minority carrier injection into the base region while monitoring the $V_{GB}$-$I_B$ characteristic. For this experiment the drain junction was used. The dominant sources of base current in the MOST channel and base region (Fig. 5.4) represent the following mechanism:

$I_{B\text{-}2\text{-}bulk}$ -- space charge region recombination in the bulk; n=2

$I_{B\text{-}1B\text{-}bulk}$ -- quasi-neutral Base region recombination in the bulk; n=1

$I_{B\text{-}1E\text{-}bulk}$ -- quasi-neutral Emitter region recombination in the bulk; n=1

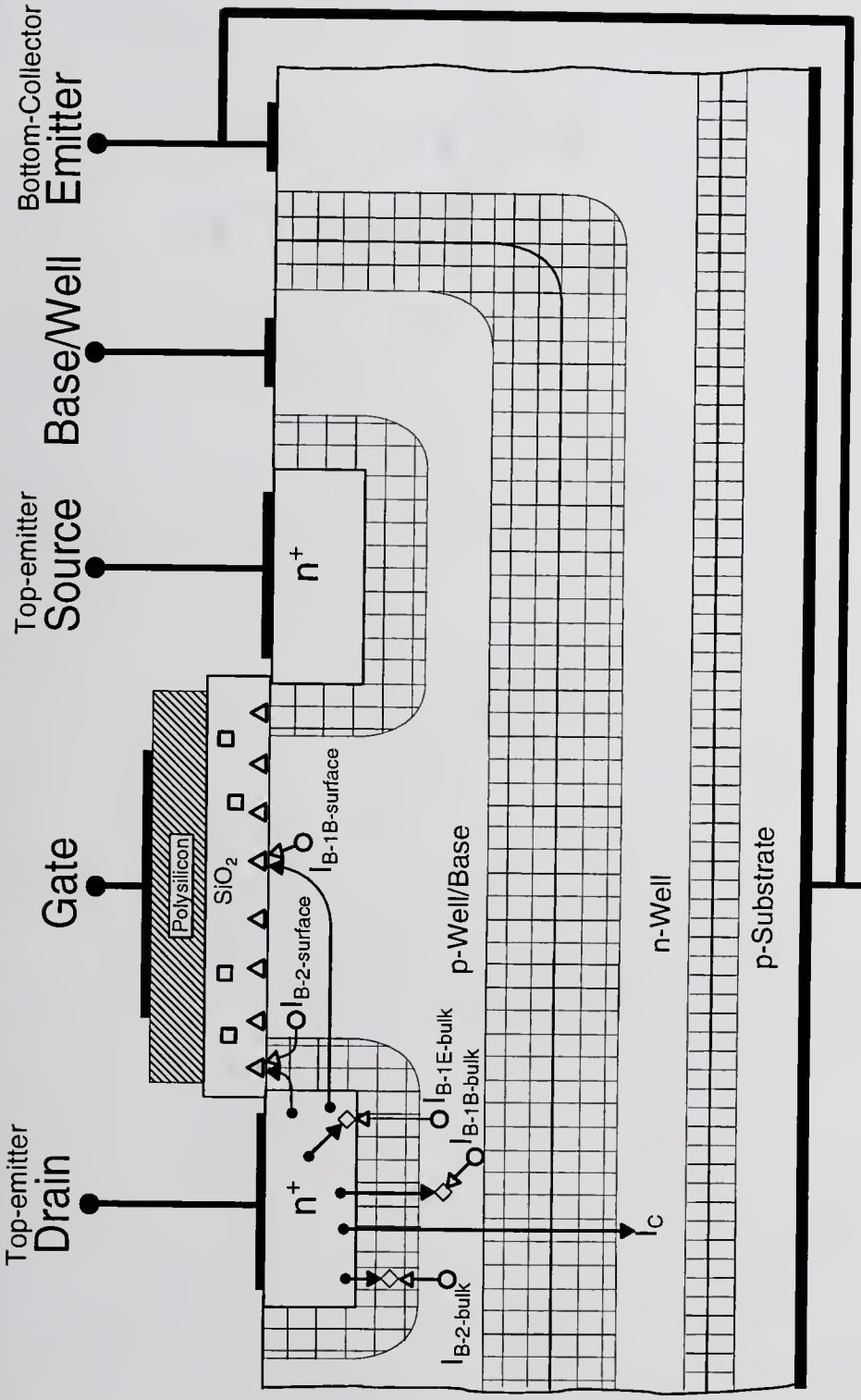



Fig. 5.4 Cross-sectional view of n-channel BiMOST illustrating the top-emitter base current measurment

$I_{B\text{-}2\text{-}surface}$ -- space charge region recombination at the surface; n=2

$I_{B\text{-}1B\text{-}surface}$ -- quasi-neutral Base region recombination at the surface; n=1

The n represents the exponential dependence of the base current ($I_B \propto \exp[qV/nk_BT]$) where n=1 is the ideal Shockley diode current, $J_1$, and n=2 is the Sah-Noyce-Shockley (generation-recombination) diode current, $J_2$ [10]. The first three sources of base recombination current are from the bulk region of the base layer and hence not modulated by $V_{GB}$ and therefore contribute only to the baseline $I_B$ level. On the other hand $I_{B\text{-}2s}$ and $I_{B\text{-}1Bs}$ will vary with $V_{GB}$ to give a peak in $I_B$ at the maximum interface recombination condition. One very important difference between the bottom-emitter and top-emitter measurement is the top-emitter's additional sensitivity to electron-hole recombination at the interface traps in the drain/base n+/p junction space charge layer, $I_{B\text{-}2s}$, when it is forward biased. In contrast, during the bottom emitter $I_B$ measurement, the $n^+/p$ drain/well and source/well junctions are at zero or reverse bias so that recombination is negligible in the drain/well and source/well junctions. Clearly, the gate bias at which maximum interface recombination occurs will differ between the space charge layer near the drain ($I_{B\text{-}2s}$) compared to the quasi-neutral p-well ($I_{B\text{-}1Bs}$) due to the difference in the surface potential of these two regions. At low forward junction bias, the $J_2$ component will dominate since most of the injected minority carriers (electrons) by the n+drain/p-well junction will recombine in the space-charge layer. Another key point is that the top emitter base current peak, due to the $I_{B\text{-}2s}$ component, is highly sensitive to the area of the space charge layer underneath the gate oxide and will therefore be influenced by the local doping impurity concentration in the p-well, such as that of the lowly-doped-drain.

The results indicate that as the oxide becomes negatively charged during the low field (1MV/cm) SHEi stress (phase-1) the $I_B$-$V_{GB}$ characteristics shift in the $+V_G$ direction and $I_{B\text{-}peak}$ also decreases significantly by almost 40% (Fig.5.5). The decreasing shift in peak base current, $\Delta I_B$, and the corresponding increase in the subthreshold $I_D$-$V_G$ swing, $\Delta S$, are shown in Fig. 5.6. The $+V_G$ shift in the $C_{inv}$-$V_G$ characteristics and the gate voltage shift for constant values of $C_{inv}$, $\Delta V_{GC}$, are also obtained and shown in Figs. 5.7 and 5.8 respectively, to illustrate the large amount of distortion in the CV during the phase-1 charging. Next, the electrons trapped at the shallow $E_C$−1eV level are field-emitted just as in the experiment presented in chapter 4. The second portion (EFSEe or phase-2) of Figs. 5.5-5.8 illustrate a complete recovery of the base current, the subthreshold swing, and the inversion layer capacitance to their original prestress values. Under the assumption that interface traps generated during phase-1 would not be annihilated during phase-2, it would appear that the distortion in $I_B$, $\Delta S$, and $C_{INV}$ are entirely due to the areally nonuniform negative charging of the gate oxide, $-Q_{OT}(y)$. The decrease in $I_B$ during phase-1 is attributed to the nonuniform negative charging of the oxide near the drain/base junction which effectively increases the concentration of holes near the $SiO_2$/Si interface and therefore reduces the space charge layer area underneath the gate where electrons and holes may recombine. This effect is illustrated by the region enclosed by the two dashed curves and dashed squares in the cross-sectional view of the drain/base junction in Fig. 5.9. The nonuniformity encountered during the $-Q_{OT}$ charging phase-1 may be attributed to a voltage drop from the center of the long channel (150μm) towards the source and drain (collector) junctions during the low field SHEi and would be proportional to $R_{CH}*I_C$. Such a

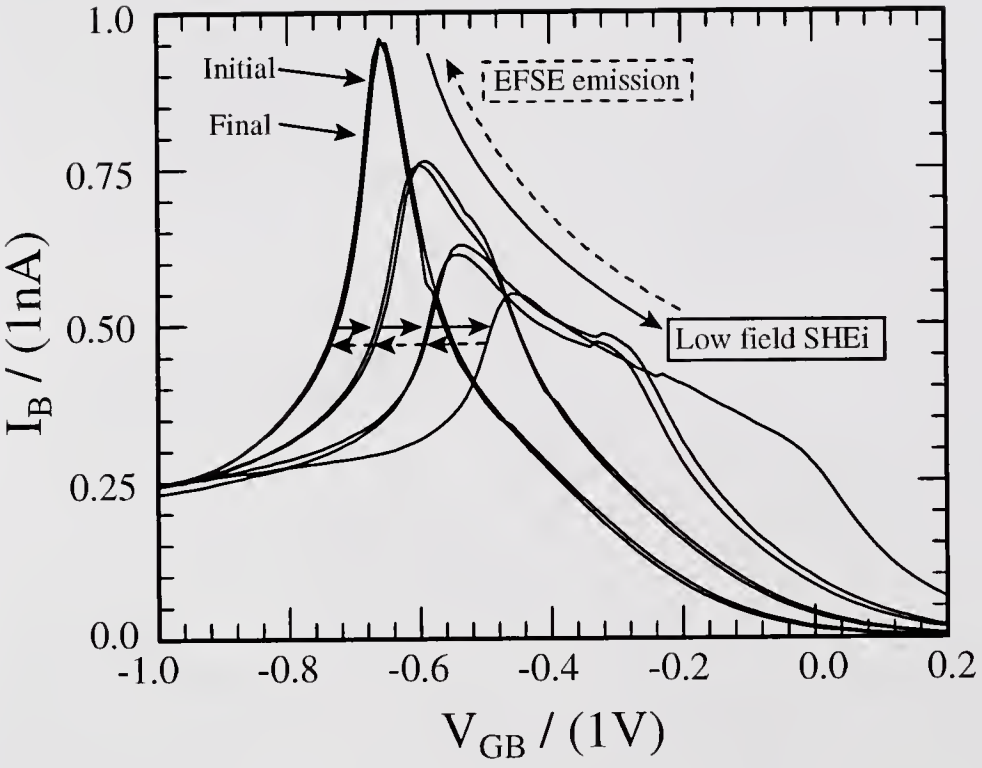



Fig. 5.5 The shift in the base current characteristics during low field (1MV/cm) SHEi stress to fill the shallow $E_C$-1eV electron traps (solid arrows), followed by EFSE emission to detrap the electrons (dotted arrows).

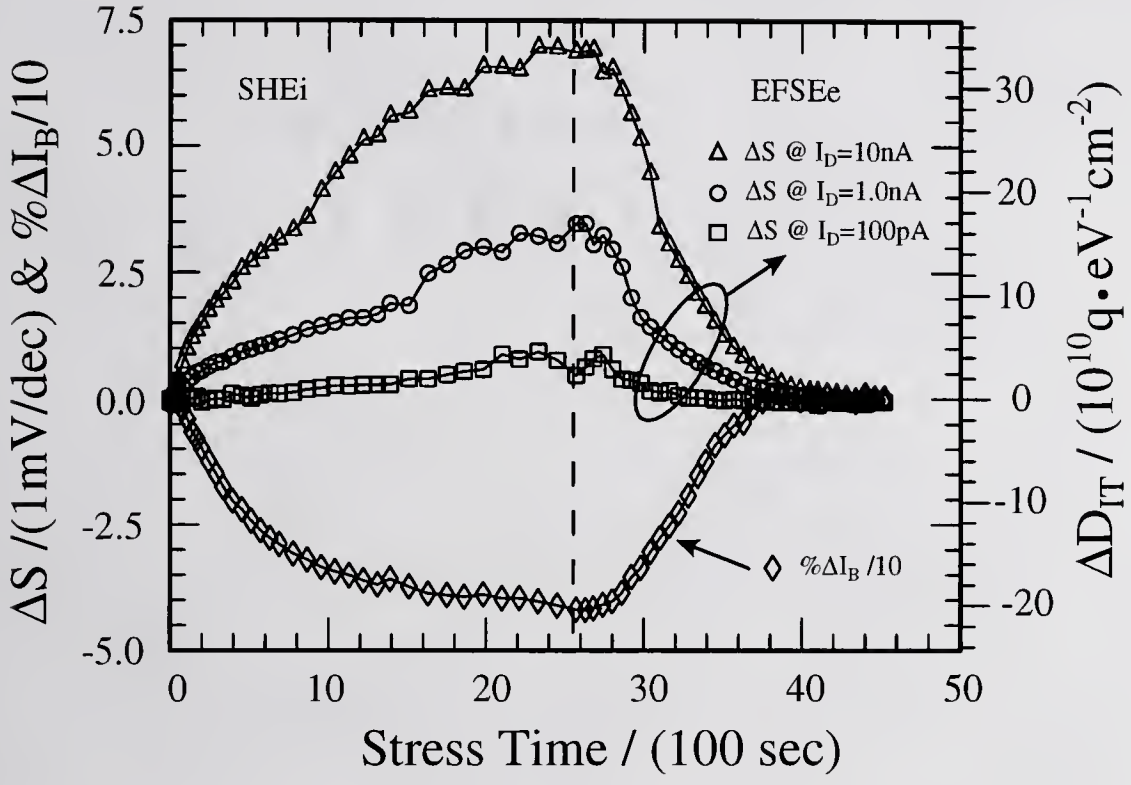



Fig. 5.6 The percent shift in the peak base current and subthreshold current swing during low field (1MV/cm) SHEi stress to fill the shallow $E_C$-1eV electron traps (left of dashed line) followed by EFSE emission to detrap the electrons (right side of dashed line).

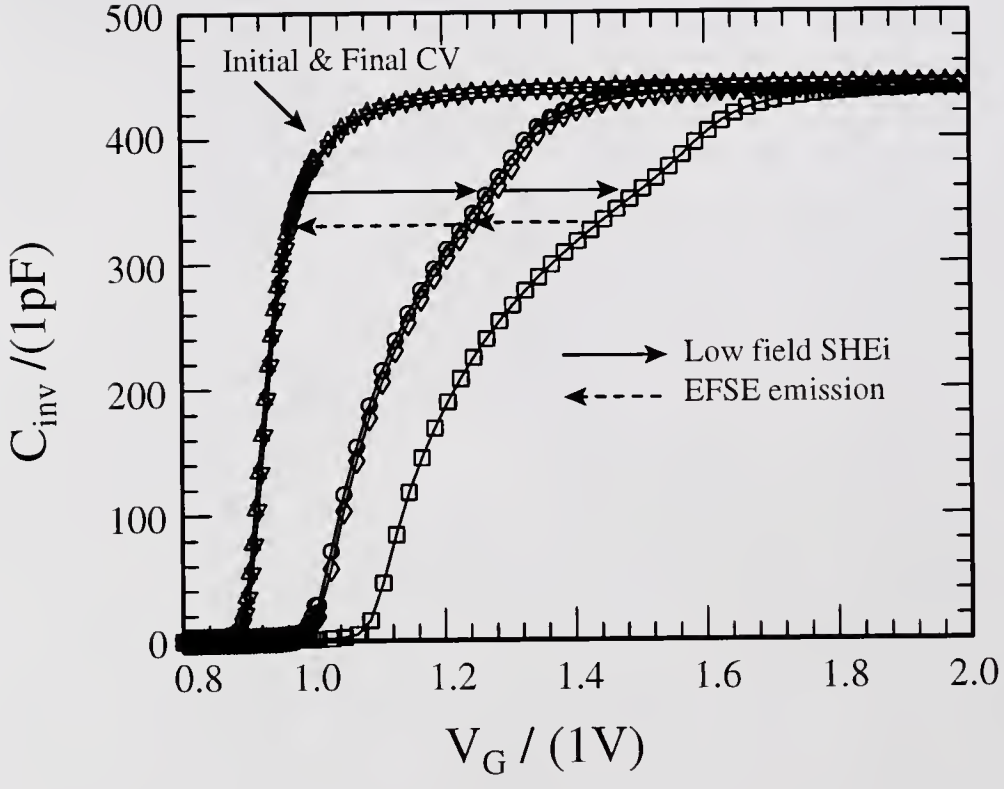



Fig. 5.7 The shift in the 10kHz inversion capacitance, $C_{inv}$ vs d.c. gate voltage, $V_G$, during low field (1MV/cm) SHEi stress to fill the shallow $E_C$-1eV electron traps (direction of solid lines) followed by EFSE emission to detrap the electrons (direction of dashed lines).

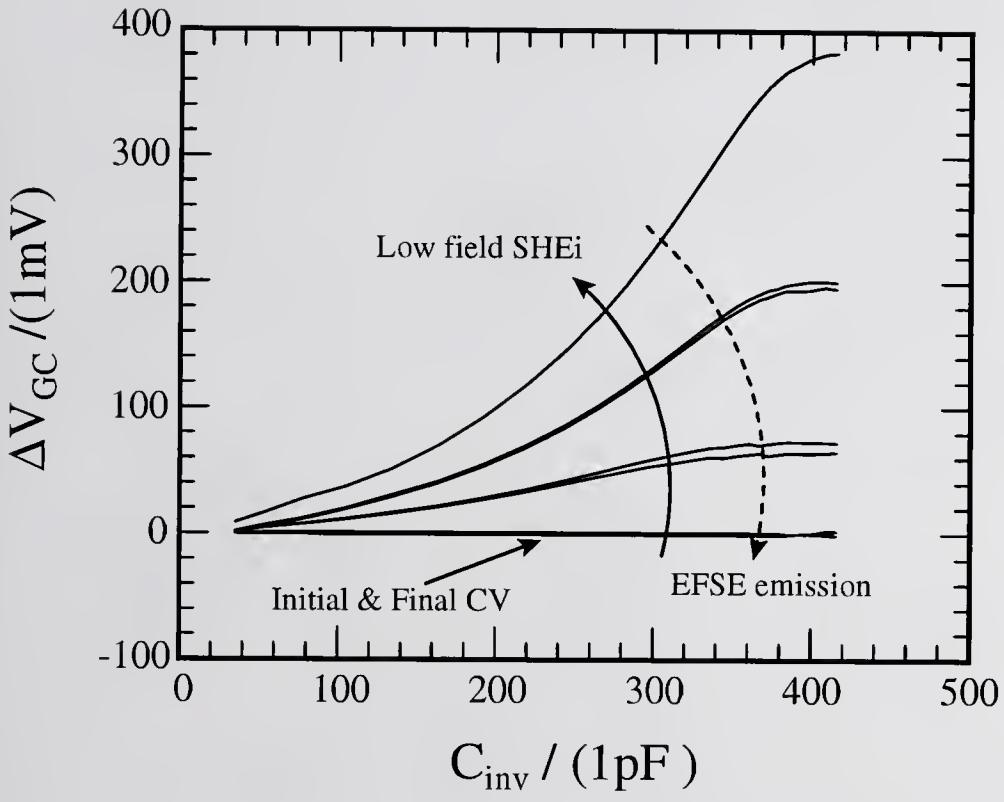



Fig. 5.8 The distortion in the 10kHz inversion capacitance, $C_{inv}$ vs d.c. gate voltage during low field (1MV/cm) SHEi stress to fill the shallow $E_C$-1eV electron traps (direction of solid arrow) followed by EFSE emission to detrap the electrons (direction of dashed dashed).

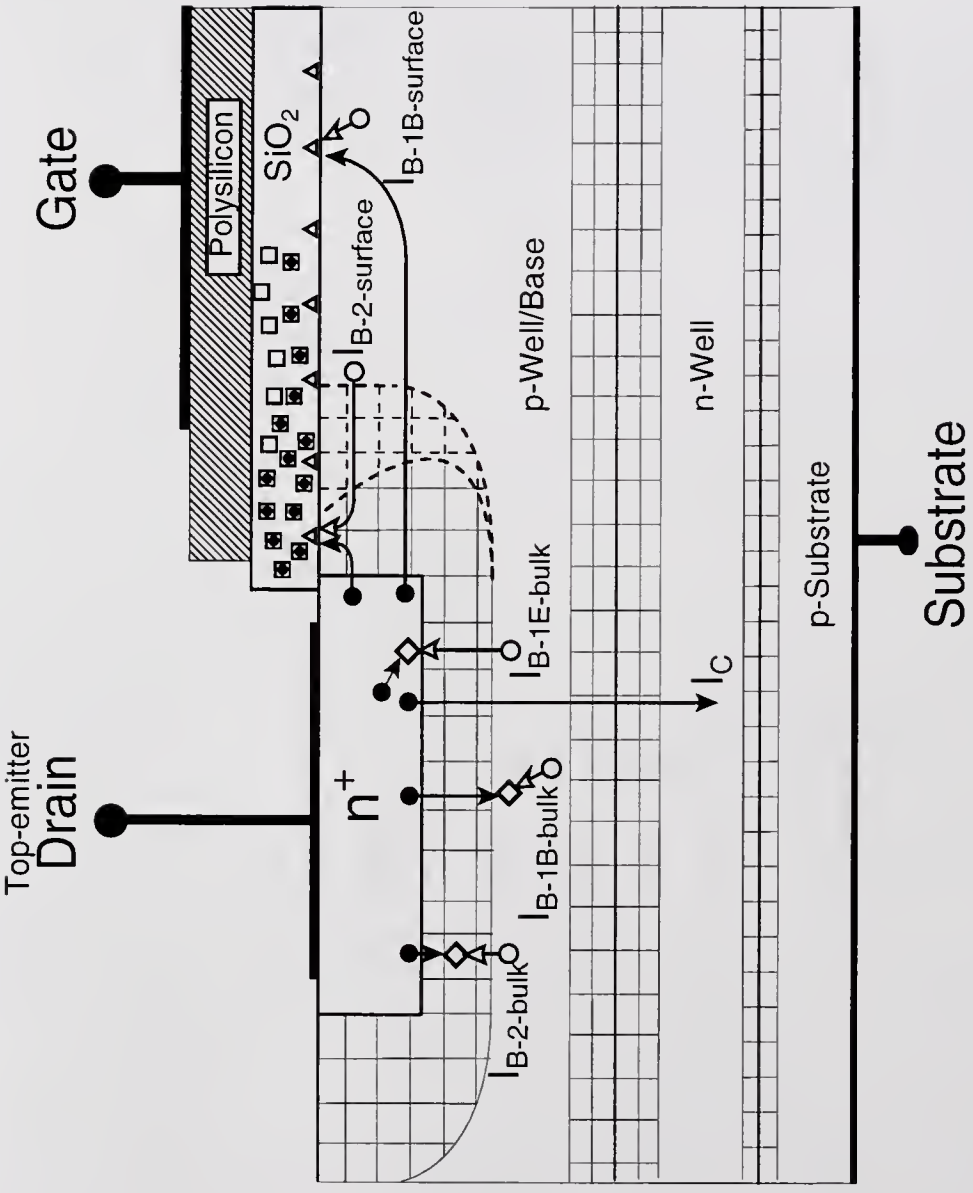



Fig. 5.9 Cross-sectional view of n-channel BiMOST illustrating the top-emitter base current measurment and the reduction in area at the $SiO_2$/Si (dashed region) following low field SHEi.

voltage drop would significantly alter the accelerating electric field profile in the silicon, $E_S$, and hence result in an areally nonuniform injection profile.

In this chapter a new and highly sensitive methodology for detecting and separating areal nonuniformity in the oxide charge distribution from the stress-generated interface traps was demonstrated [59]. The methodology employed the two measurements: 1) the new DCIV method recently proposed by Neugroschel and Sah [12] to detect the stress-generated interface traps by measuring the $I_B$ of the BiMOST, and 2) the traditional subthreshold dc $I_D$-$V_G$ swing to detect both the stress-generated interface traps and nonuniform oxide charge distributions. The methodology was demonstrated in five SAM experiments performed on five BiMOSTs where spatially uniform and nonuniform (from source to drain) oxide charge distributions were generated by experiments using the two FNTEi polarities, in two SHEi/CHEi experiments with $V_{DS}$=0 and $V_{DS}$=4V, and by low field SHEi at 77°K. The increased distortion of the a.c. $C_{inv}$-$V_G$ characteristics during the low field SHEi for $-Q_{OT}$ charging and its complete recovery provided further support to the new combined d.c. $\Delta S$ and DCIV measurement methodology proposed in this chapter.

# CHAPTER 6
# CURRENT-ACCELERATED CHE STRESS FOR RAPID TIME-TO-FAILURE EXTRAPOLATION

Thus far the injection stress applied to the n-BiMOST's in this study included FNTEi, SHEi and SHEi/CHE. This chapter compares the results of the conventional voltage-accelerated CHE and the new current-accelerated CHE stressing methodologies and their effect on the channel mobility, the drain saturation current, the gate threshold voltage and the DCIV peak base current. The traditional time-to-failure (TTF) extrapolation by voltage-accelerated CHC stress will also be reviewed to illustrate its limitations and to point out the advantages of the current-accelerated methodology.

## 6.1 Conventional Channel Hot Carrier Stress

The voltage-accelerated channel hot carrier (CHC) stress methodology, for n-channel and p-channel MOST's has become an industry standard for extracting the time-to-failure (TTF) of MOST's to assess the reliability of new technologies at lower operation voltages. The customary CHC stress condition is to apply $V_D \cong 2.5V_G$, so that the channel is strongly depleted at the drain, and the substrate (the well in MOST's or base in the BiMOST) current is maximized during stress. To avoid confusion with the

base current measurement ($I_B$-$V_{GB}$) used to characterize interface states in the previous two chapters the substrate current will be denoted by the standard notation $I_X$ (or $I_{SUB}$) although they are the very same current measured at the same terminal, B, X, or W (Well), but at different bias configurations. The substrate current component originates from the impact generation of electron-hole pairs by energetic electrons transiting through the high-field space-charge region of the reverse biased drain/base junction (Fig. 6.1). The inversion electrons entering the channel at the source drift through the inversion channel until they reach the drain-junction space-charge layer where they are then accelerated by the high electric field to high kinetic energies. If the electron kinetic energy gained is more than 1.2eV, as recently demonstrated theoretically and experimentally by Lu and Sah [62], before exiting the drain, the electrons can impact release an electron-hole pair. The negative sign of $I_X$ arises from the impact-generated holes exiting through the p-well contact. Furthermore, if these energetic electrons gain enough kinetic energy (3.1eV) they may also be injected into the oxide to give negative [56,57] or positive [56, 61, 62] charge as demonstrated in the preceding chapters, or to break the weak interfacial bonds, such as the Si-H and SiO-H discussed by Sah [9], and create an interface state, $Q_{IT}$.

Typical $I_X$-$V_{GS}$ characteristics, with $V_{DS}$ as the parameter, taken on the $100\times100\mu m^2$ n-channel BiMOSTs used in this study, are shown in Fig. 6.2. These conventional CHE curves illustrate the limiting nature of this technique when extrapolating TTF at low operating voltages ($V_D$ and $V_G$) within a reasonable measurement time of 150 hours or less (<5 days). The conventional approach therefore is to accelerate the stress by raising the voltages and corresponding kinetic energy of

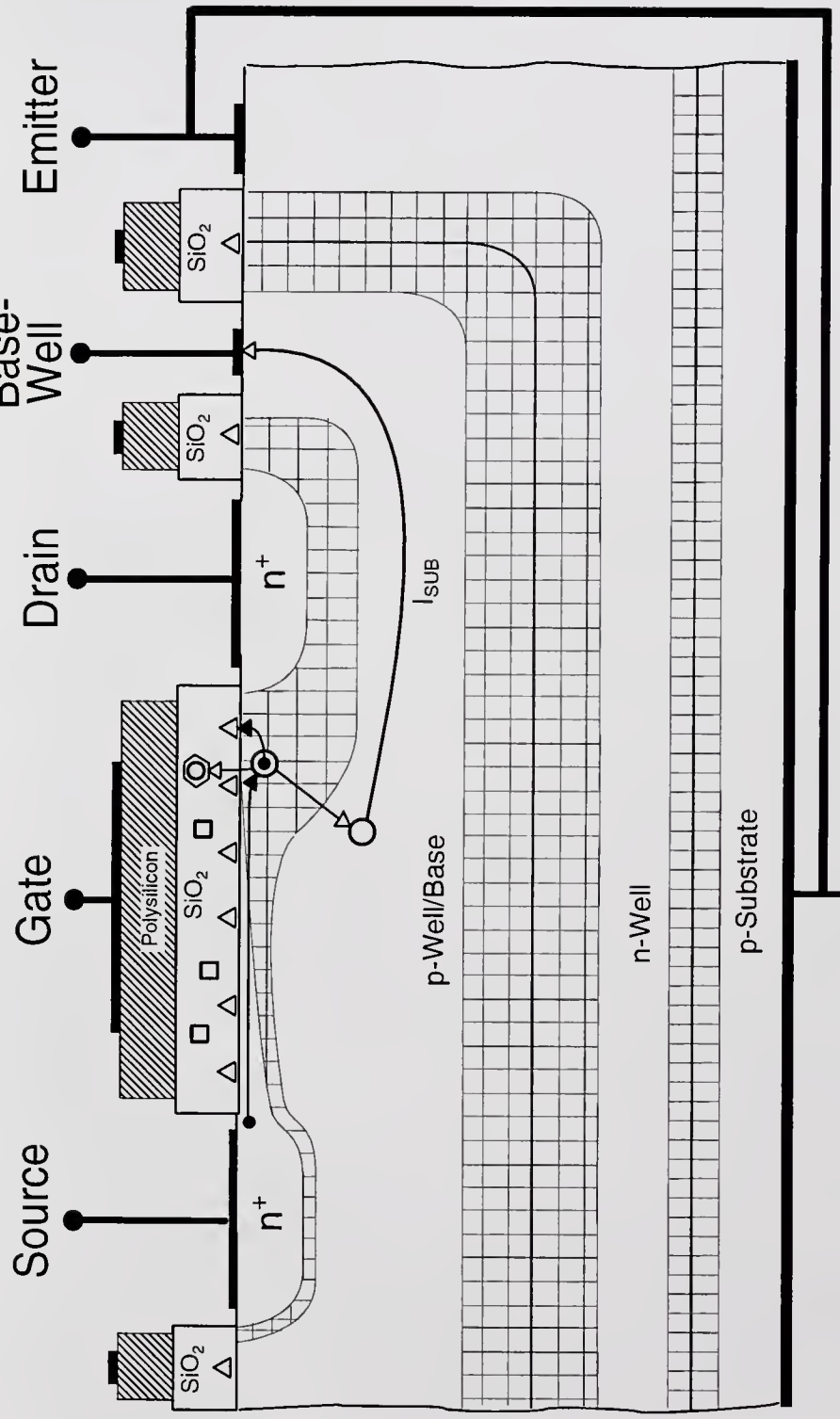



Fig. 6.1 Cross-sectional view of an n-channel BiMOST illustrating the CHEi stress and the electron impact ionization of electron-hole pairs.

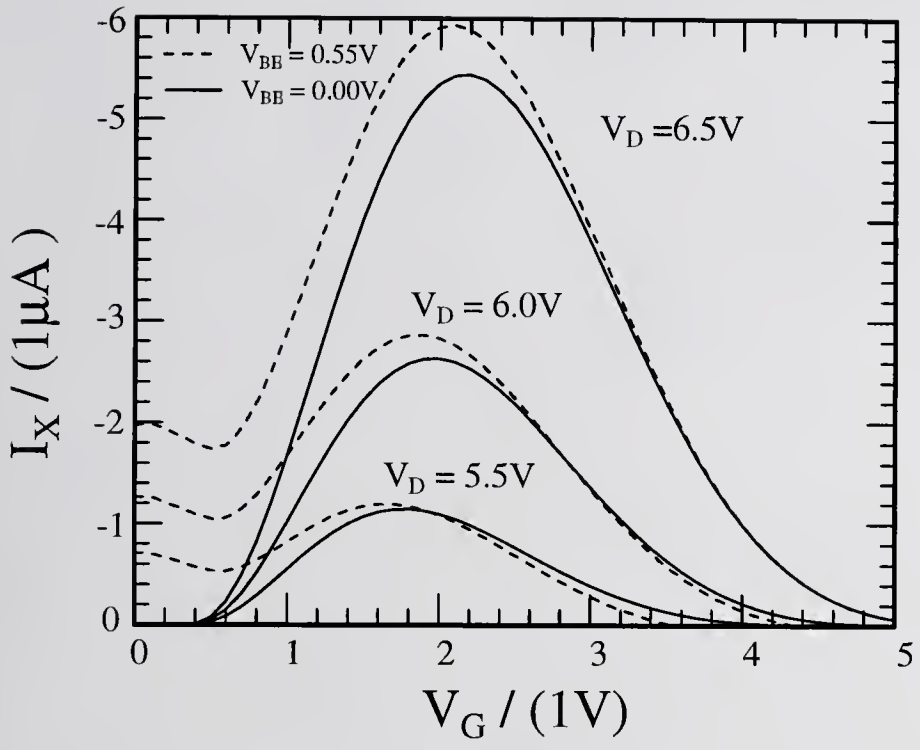



Figure 6.2 Substrate hole current, $I_X$, versus gate bias at $V_D$=5.5-6.5. The dotted lines represent bottom-emitter current-accelerated data with $V_{BE}$=0.55V

the carriers responsible for the damage at the $SiO_2$/Si interface. In doing so it is incorrectly assumed that the microscopic failure mechanisms are independent of the spatial and kinetic energy distributions of the carriers (electrons in the nMOST). Clearly therefore the traditional voltage-acceleration method is not reliable for extrapolating TTF in future deep submicron technologies operating at voltages below 2V as will be shown by the results in the next section.

## 6.2 Bottom-Emitter Current-Accelerated CHE

Recently Neugroschel and Sah proposed two current acceleration techniques [12,13] for extrapolating the operation TTF at low voltages in BJT with stress-time acceleration greater than 100. In this thesis a similar current-acceleration method for CHE TTF extrapolation is demonstrated for the first time on nMOSTs. The current-acceleration for MOSTs exploits the unique vertical bipolar structure of the BiMOST test structure by forward biasing the bottom-emitter/base junction. The forward biased minority carriers (electrons in nMOST of this study) diffuse through the base layer towards the $SiO_2$/Si surface where they are swept across the channel inversion layer along with the carriers originating from the source junction (Fig. 6.3). Hence the stress due to the impact generation of electron-hole pairs occurring near the drain is current-accelerated by the larger electron flux that enters the high-field space-charge layer near the $SiO_2$/Si surface. More important, the kinetic energy distribution of these additional electrons is the same as those in the nonaccelerated CHC case since the $V_D$ and $V_G$ are kept constant. The alteration of the channel accelerating electric field distribution by

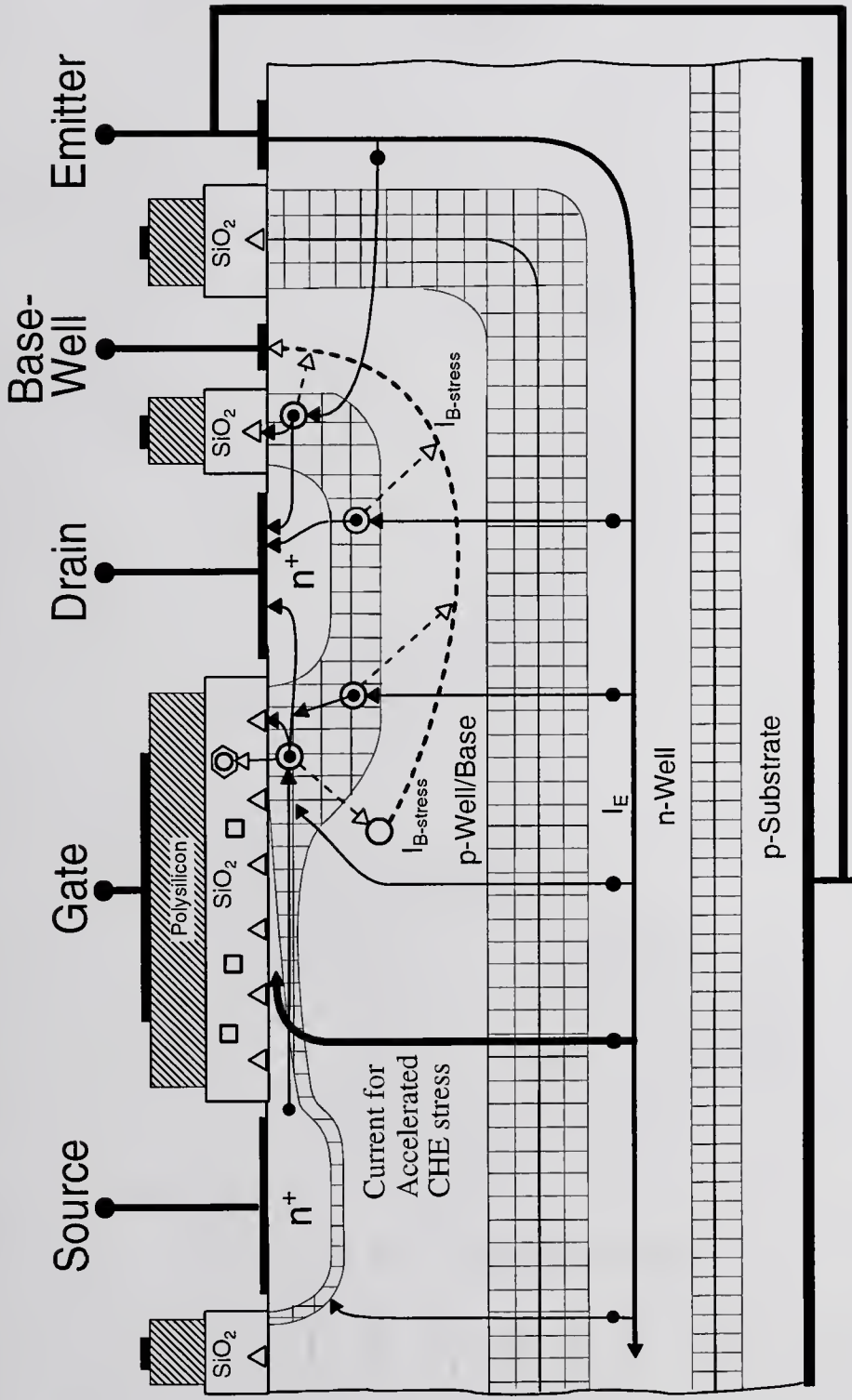



Fig. 6.3 Cross-sectional view of n-channel BiMOST illustrating the CHEi stress with the current-acceleration component labeled by the dark $I_E$ current line.

the injected electrons is expected to be small. It is noted however that because of the diffused emitter geometry of this n-BiMOST structure there is a significant contribution to the drain current from electrons entering the drain through its bottom-facing junction and entering laterally near the surface outside the channel. Furthermore, there will be additional impact generation of electron-hole pairs occurring in the bulk (bottom-facing part) of the drain/base junction space-charge layer and near the surface outside the channel. These secondary sources of drain current will increase $I_X$ during stress but will not damage (or create interface traps at) the $SiO_2$/Si interface in the channel. The secondary surface impact generation current component outside the channel will however increase the baseline of the $I_B$ current (DCIV) by creating interface traps in the oxide layer adjacent to the drain. However, the surface potential in the location of these interface states will not be modulated by the gate bias when measuring the $I_B$-$V_{GB}$ characteristic and therefore will not exhibit the peak behavior like the interface states in the channel. The increase in $I_D$ when $V_{BE}\neq 0$ is easily demonstrated by the $I_{DS}$-$V_{DS}$ family of curves with $V_{GS}$=1-3V and $V_{BE}$=0-0.55V as secondary variables in Fig. 6.4. The value of the accelerating emitter current is also shown in Fig.6.4.

The change in the top-emitter (drain) DCIV characteristics, $\Delta I_B$, during CHE stress ($V_D$=8V, $V_G$=2.8V and $V_{BE}$=0.0V) for the 100x100$\mu m^2$ n-BiMOST are shown in Fig. 6.5. The value of the accelerating reverse bias voltage on the drain/base junction is $V_{DS}$ - $V_{DSsat}$ = $V_{DS}$ – ($V_{GS}$ – $V_{GT}$) ≃ 8–(2.8–0.5) = 5.7V. Though the peak near the flatband voltage or $V_{GB}$ ≃ – 0.38V is unaffected during the CHE stress, an increasing secondary $I_B$ peak is observed in the accumulation portion of the $I_B$-$V_{GB}$ curve,

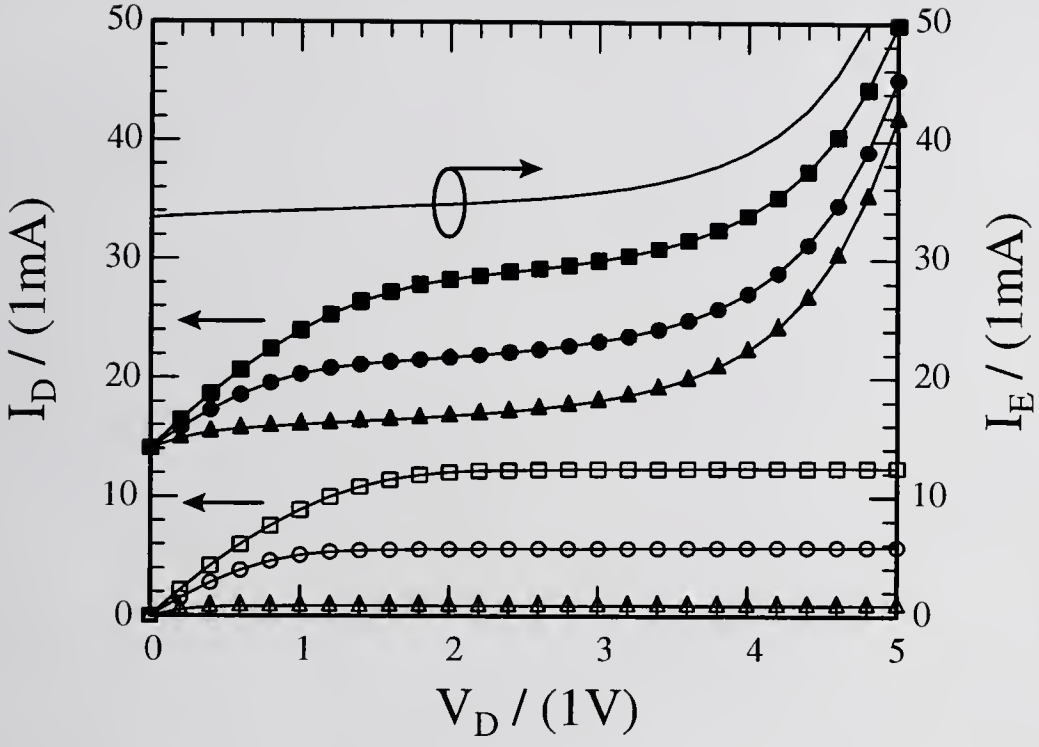



Figure 6.4 Drain current vs drain voltage for $V_G$=1, 2, 3 volts. The solid marker curves represent the current-accelerated data with $I_E$ (solid line without marker) plotted on the right axis.

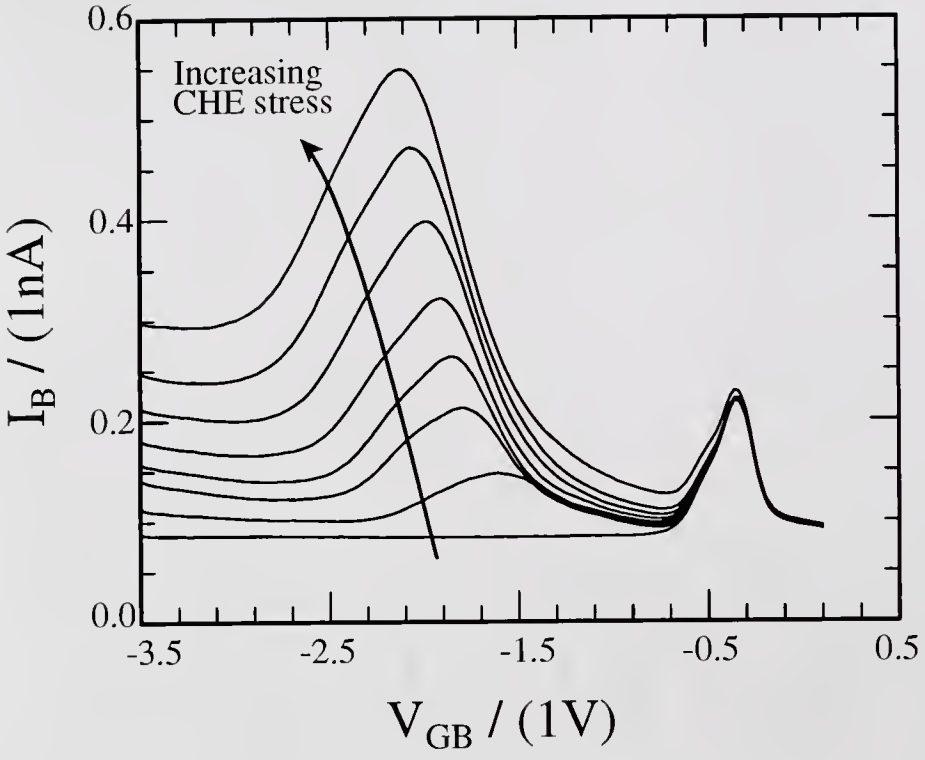



Figure 6.5 The top-emitter DCIV characteristics versus CHE stress for an n-BiMOST. The stress conditions were $V_D$=8V and $V_G$ =2.8V.

indicating a large build-up of interface states near the drain junction. The percent increase in $I_B$ of this secondary peak is plotted in Fig. 6.6 versus the drain fluence, $N_{INJ} = (1/qZ)\int I_D dt$. The corresponding gate voltage shift of the secondary $I_B$ peak is plotted in Fig. 6.7 illustrating a large −0.7V shift in the local threshold voltage near the drain/base junction due to the build-up of $Q_{IT}$ and possibly $+Q_{OT}$. It is also evident that the microscopic failure mechanisms responsible for the $\%\Delta I_B$ are limited as indicated by the saturating nature of both the $\%\Delta I_B$ and the $\Delta V_{G\text{-}IBpeak}$ curves. Hence the empirical and statistical linear or log-log TTF extrapolation methodology traditionally used in industry for estimating the damage at long CHE stress times is clearly in error.

Next the drain bias was kept constant ($V_D$=8.0V) while the gate bias was varied between $V_G$ = 2.8V and 4.1V so that the accelerating bias near the drain/base junction was varied between $V_{DS}-V_{DS\text{-}sat}$ = 5.7V to 4.4V. The increase in $\%\Delta I_B$ vs $N_{INJ}$ for the three $V_G$ values with $V_D$ = 8.0V is plotted in Fig. 6.8 showing a large variation in the saturation values. As the reverse bias field near the drain decreases so does the damage or interface trap generation as exhibited by the $\%\Delta I_B$ data which would indicate that there is a threshold voltage beyond which the damage becomes negligible. Hence the empirical-statistical linear or log-log TTF extrapolation to lower operating voltages traditionally used in industry is also in error.

A second set of CHE stress and measure (SAM) experiments were conducted for low $V_G$ = 0.9V and $V_D$ = 5V to 8V, with and without the current-acceleration from the forward-biased bottom-emitter. The $\Delta I_B$ vs stress time for $V_G$ = 0.9V, $V_D$ = 6.0V and varying degrees of current-acceleration, as controlled by the current-limited forward bias applied to the bottom emitter/base junction, $V_{BE}$ = 0.0V to 6.0V, are shown in Fig.

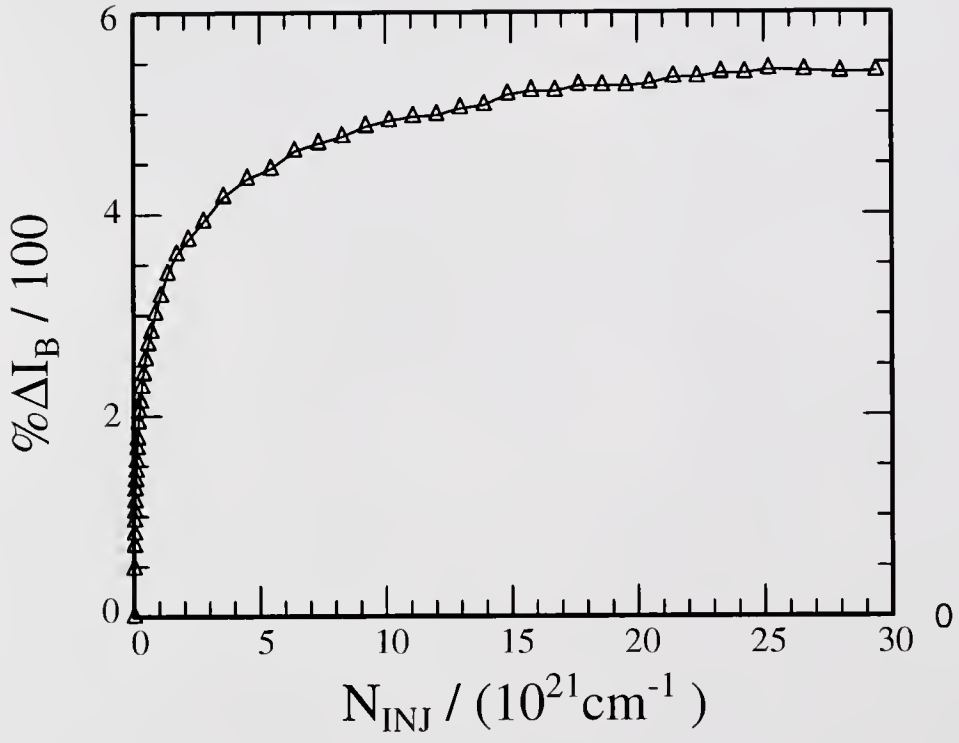



Figure 6.6 Percent increase in the top-emitter DCIV secondary $I_{B\text{-}peak}$ value versus the drain fluence during CHE stress.

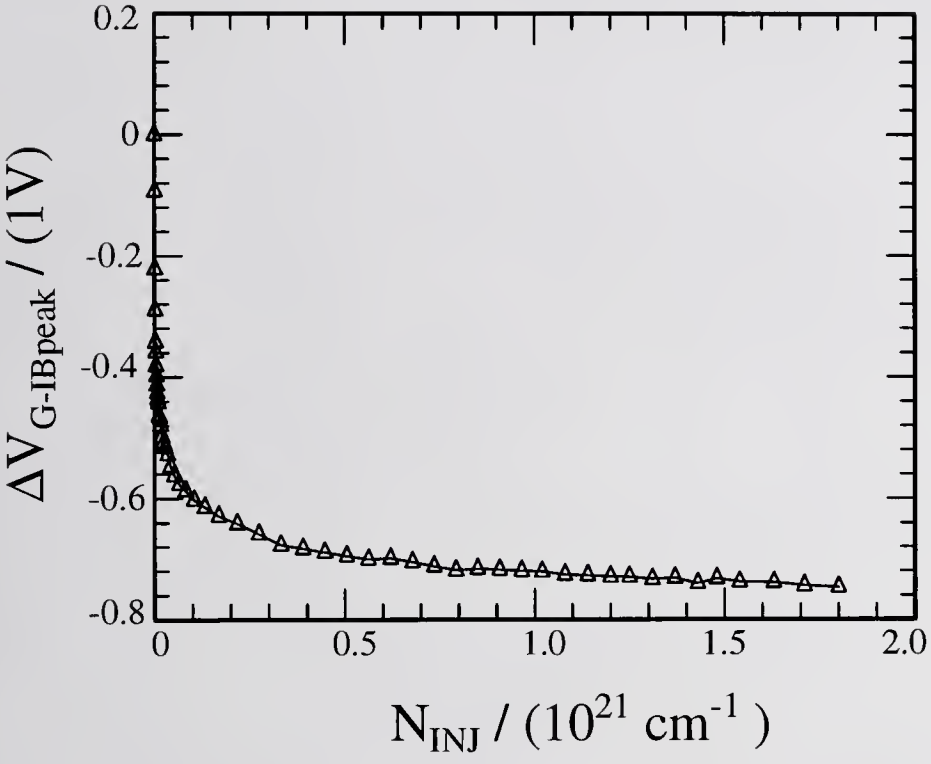



Figure 6.7 Gate voltage shift in the peak value of the base current measured by the top-emitter DCIV method.

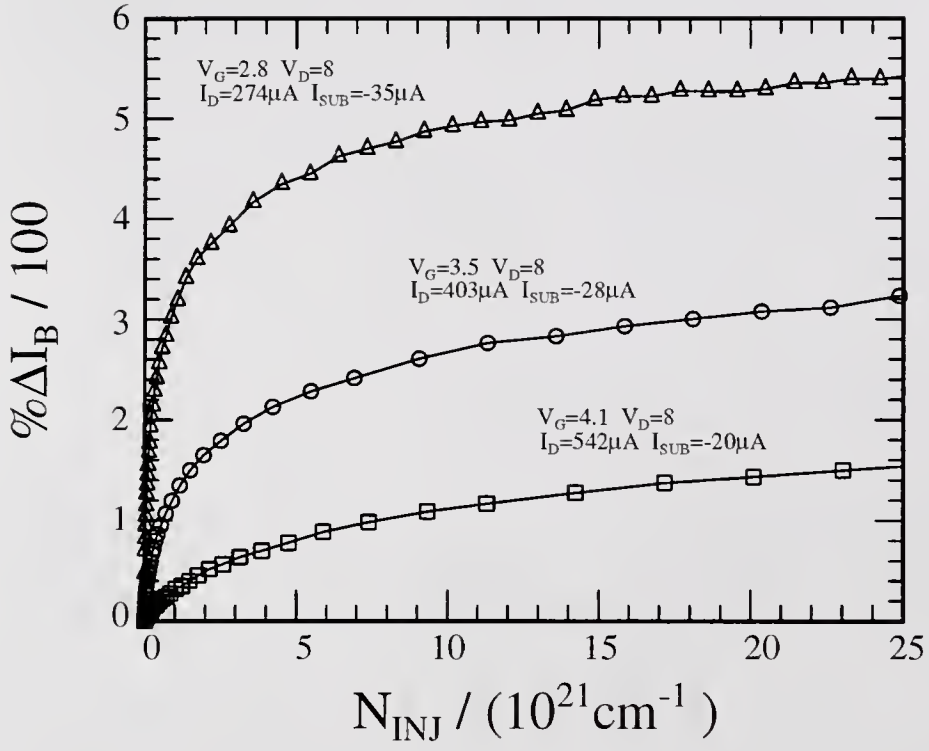



Figure 6.8 Percent increase of the top-emitter DCIV secondary $I_{B\text{-}peak}$ versus the drain fluence during CHE stress.

6.9a. As indicated in this figure, for increasing current-acceleration (increasing $V_{BE}$ or $I_E$) the $\Delta I_B$ degradation is accelerated by as much as 100 times. When increasing $V_{BE}$ between 2.5V and 6.0V it appears that the degradation may have actually decreased slightly. This can be attributed to an increase in the baseline of the $I_B$ current in the surface outside the channel region as discussed earlier in this section. If the data is adjusted to account for this increase in the baseline $I_B$ the two curves coincide quite well as indicated in Fig. 6.9b. The remainder of the data presented in this chapter will therefore be adjusted to account for this effect.

Nevertheless, it appears that the current-acceleration due to the additional $I_D$ contribution from the bottom-emitter is limited beyond $V_{BE}$=2.5 or $I_D$=2.9mA possibly due to current crowding at the surface. Any additional current flowing through the drain beyond this value (2.9mA) must therefore be collected by the peripheral bulk area of the drain/base junction as opposed to the inversion channel at the $SiO_2$/Si interface. As mentioned earlier this current will not contribute to the $\Delta I_B$ damage except by increasing the baseline $I_B$ since it is not flowing along the channel area. This is evident in Fig. 6.10 which replots the $\Delta I_B$ data of Fig. 6.9b versus the drain fluence. The non-accelerated data has now merged with the current-accelerated data for $V_{BE}$=0 to 2.5V which supports the theory that the kinetic energy of the carriers in the current-accelerated case has not changed as would have been the case using voltage-acceleration. The high $V_{BE}$=6.0V case does not merge with the other three lower forward-bias curves because the drain fluence has the additional contribution from the peripheral bulk drain current just mentioned. The merging of the curves in Fig. 6.10 is also consistent with the fact that the drain current as well as the substrate current ratios

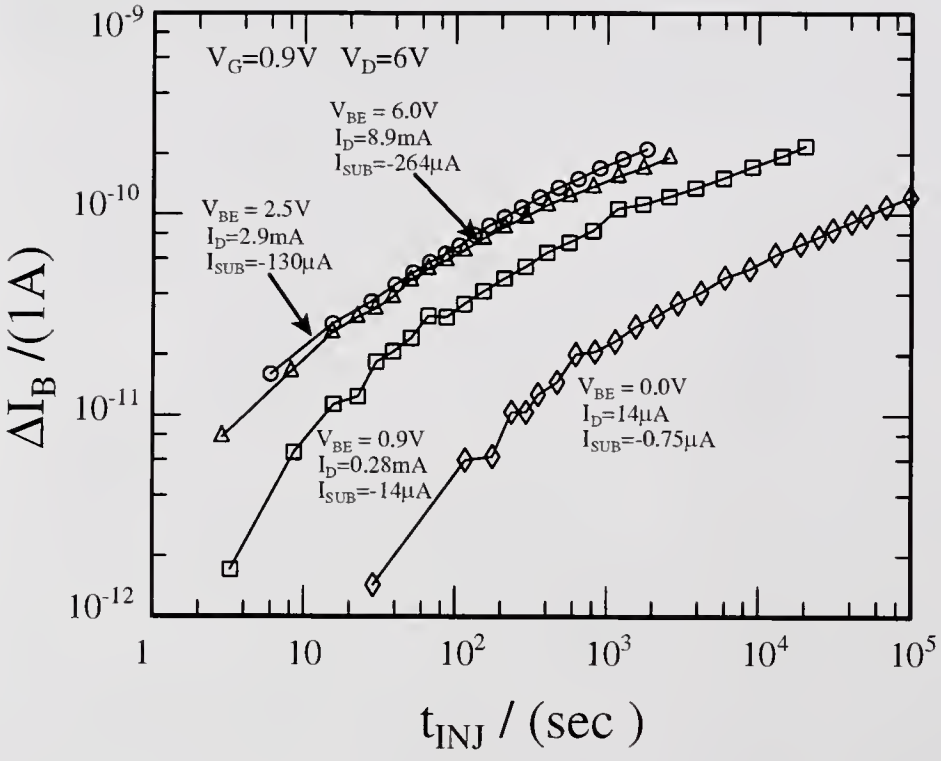



Figure 6.9a Increase of the top-emitter DCIV secondary $I_{B\text{-}peak}$ versus the total injection time during CHE stress.with varying degrees of bottom-emitter current-acceleration.

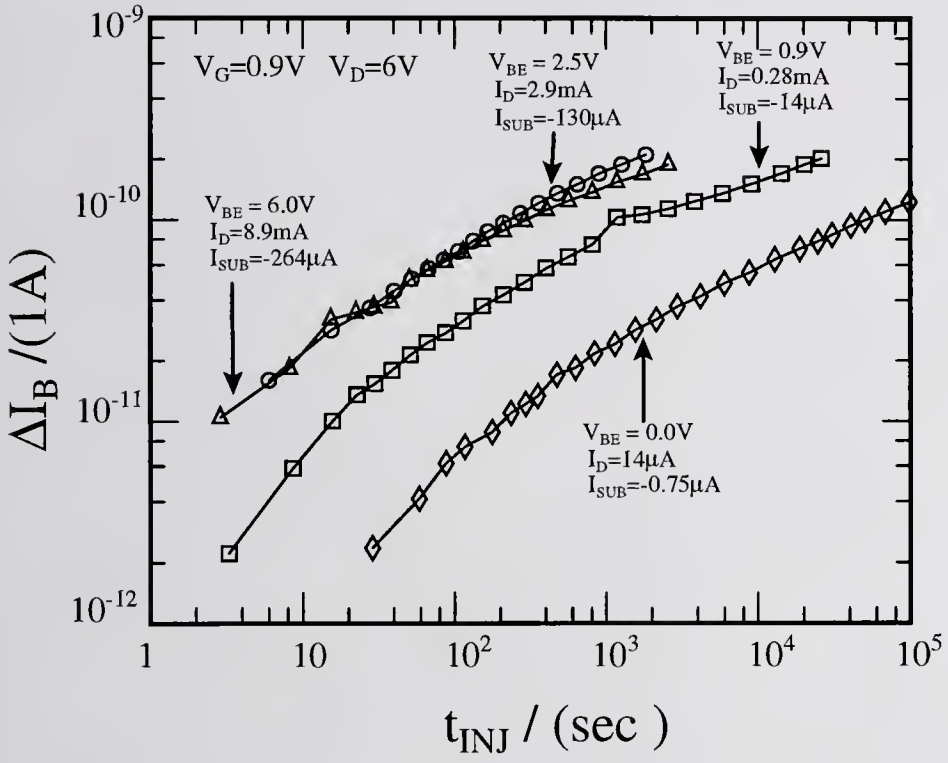



Figure 6.9b Increase of the top-emitter DCIV secondary $I_{B\text{-}peak}$ versus the total injection time during CHE stress.with varying degrees of bottom-emitter current-acceleration. The data has been adjusted by the baseline $I_B$ value..

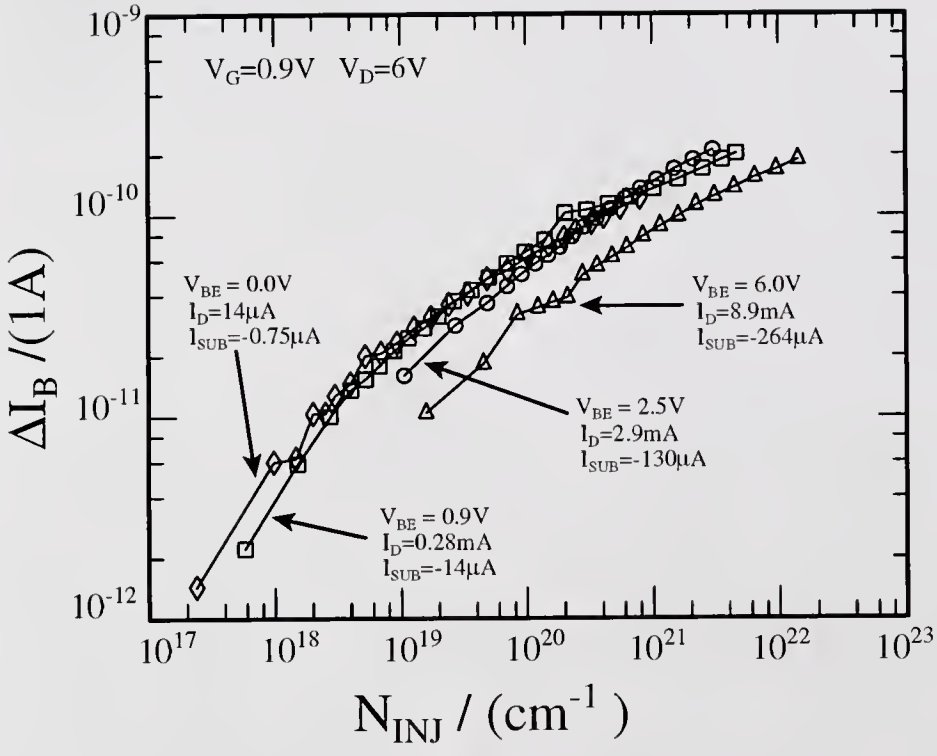



Figure 6.10 Increase of the top-emitter DCIV secondary $I_{B\text{-}peak}$ versus the total drain fluence during CHE stress.with varying degrees of bottom-emitter current-acceleration.

before and after acceleration are proportional to the amount of the acceleration. For example the acceleration factor between $V_{BE}$ = 0V to 0.9V is approximately 20 while $I_{D\text{-}acc}/I_D$ = 280μA/14μA = 20 and $I_{X\text{-}acc}/I_X$ = 14μA/0.75μA ≈ 19; where $I_{X\text{-}acc}$ and $I_X$ are the accelerated and non-accelerated values. The same good agreement is also found for the 8-10 times acceleration range between $V_{BE}$ = 0.9 to 2.5V where $I_{D\text{-}acc}/I_D$ ≈ 10.4 and $I_{X\text{-}acc}/I_X$ = 9.3. However, the excess accelerating current flow will modulate the base carrier concentration and produce a 2-D resistive voltage drop in the base region which in turn will alter the field profile near the drain/base and the source/base junctions. Collectively these effects are evidenced by the $-\Delta V_{GT}$ of the device (Fig. 6.4) which may also account for the divergent or non-parallel shift of the $V_{BE}$=2.5V and $V_{BE}$=6.0V stress curves at high $t_{INJ}$ (Fig. 6.9b) since a $-\Delta V_{GT}$ would reduce the value of $V_{D\text{-}dep} = V_{DS} - (V_{GS} - V_{GT})$ and correspondingly the field near the drain/base junction.

Now that the functionality of the bottom emitter current-acceleration method in MOST's has been illustrated the TTF and QTF (charge to failure) will be extracted for $V_G$ = 0.9V, $V_{BE}$ = 0 and 2.5V and a range of $V_D$ = 5V to 8V. The charge to failure is calculated from the drain fluence measured in these experiments. Since the $\Delta V_{GT}$, $\Delta I_{D\text{-}sat}$, $\Delta \mu_{neff}$ degradation for these large 100×100μm$^2$ devices was too small (<0.1% change) the 100% $\Delta I_B$ value was used as the TTF and QTF criteria in Figs. 6.11 and 6.12 respectively. The TTF data illustrate a varying amount of acceleration which appears to increase at lower values of $V_D$. The QTF data on the other hand merges at the lower $V_D$ stress voltages but deviates for $V_D > 6V$ or $V_D - V_{D\text{-}sat} = 5.6V$. One reason for the deviation at higher voltages may be due to the introduction of another failure mechanism because of the two dimensional nature of the injection near the drain when

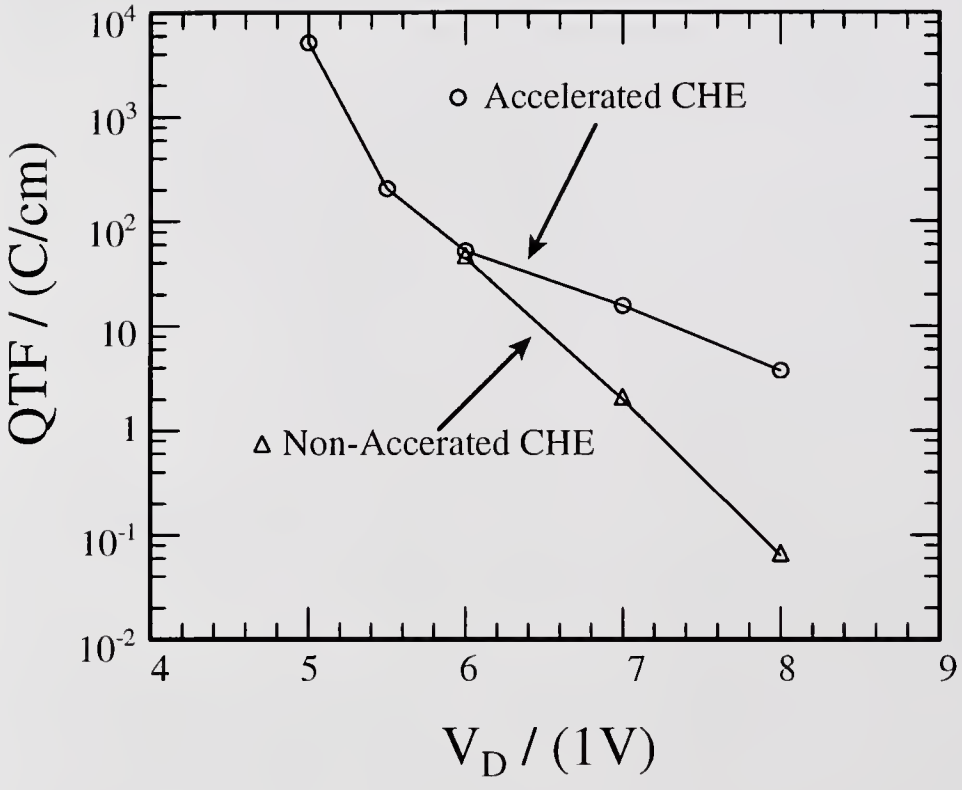



Figure 6.11 Charge to failure measured at 100%$\Delta I_B$ during CHE stress with $V_G$=0.0V and $V_{BE}$=0 for the non-accelerated data and $V_{BE}$=2.5V for the accelerated data.

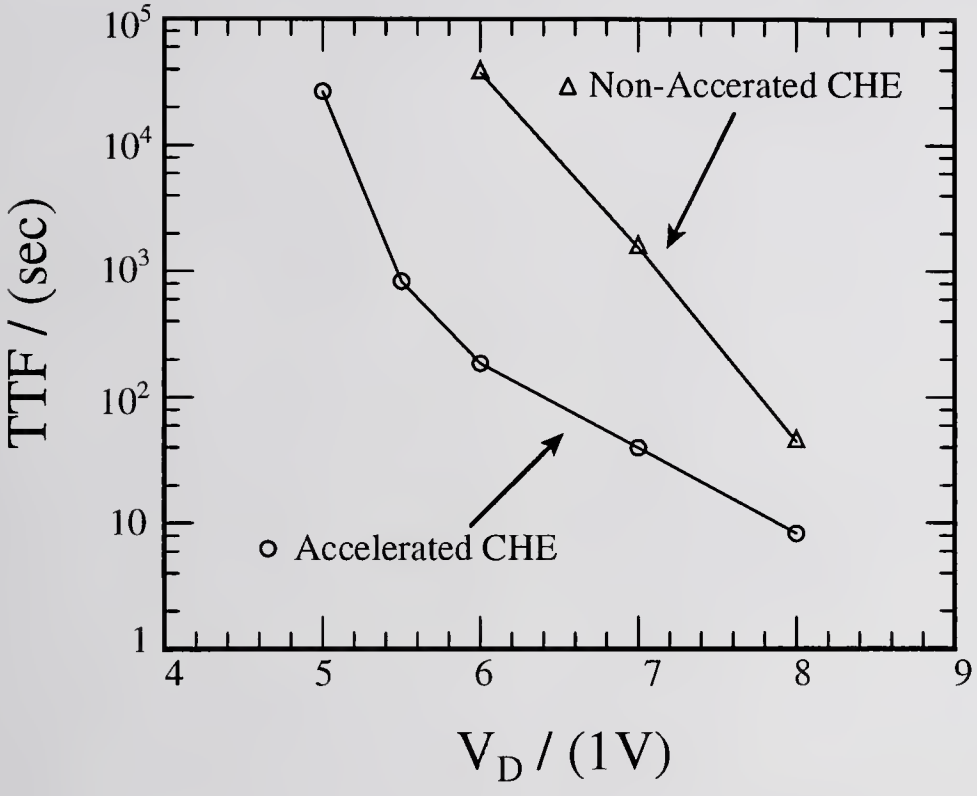



Figure 6.12 Time to failure measured at 100%$\Delta I_B$ during CHE stress with $V_G$=0.0V and $V_{BE}$=0 for the non-accelerated data and $V_{BE}$=2.5V for the accelerated data.

using the bottom emitter to accelerate the stress. In fact at high enough reverse bias across the drain/base junction it would not be unlikely to have SHEi occurring near the drain. Another factor which may be responsible is the spatial distribution of $Q_{IT}$ or $Q_{OT}$ near the drain since the top-emitter DCIV measurement was shown to be sensitive to areal inhomogeneity in addition to $\Delta D_{IT}$ in chapter 5.

## 6.3 Top-Emitter Current-Accelerated CHE

An alternative approach to the bottom-emitter current-acceleration method just demonstrated for long-channel nBiMOSTs is to forward bias the source junction during the CHE stress, as suggested by Sah. The results of this measurement, shown in Fig. 6.13, exhibit a very limited amount of acceleration when $V_{SX} = -1.0V$, $V_{GX} = 0.9V$ and $V_{DS} = 7V$ compared to the previous condition of $V_{SX} = 0V$, $V_{GX} = 0.9V$ and $V_{DS} = 7V$. The limited acceleration in this case is most likely due to the lower voltage drop in the depleted drain space-charge layer since $V_{GS} = V_{GX} - V_{SX} = 0.9V - (-1.0V) = 1.9V$ so that

$$V_{D\text{-}dep}(\text{accelerated}) \equiv V_{DS} - (V_{GS} - V_{GT})$$
$$= 7V - (1.9V - V_{GT\text{-}0} + \Delta V_{GT})$$
$$= 5.1V + V_{GT\text{-}0} - \Delta V_{GT}$$

while the non-accelerated case has

$$V_{D\text{-}dep}(\text{non-accelerated}) \equiv V_{DS} - (V_{GS} - V_{GT\text{-}0})$$
$$= 7V - (0.9V - V_{GT\text{-}0})$$
$$= 6.1V + V_{GT\text{-}0}.$$

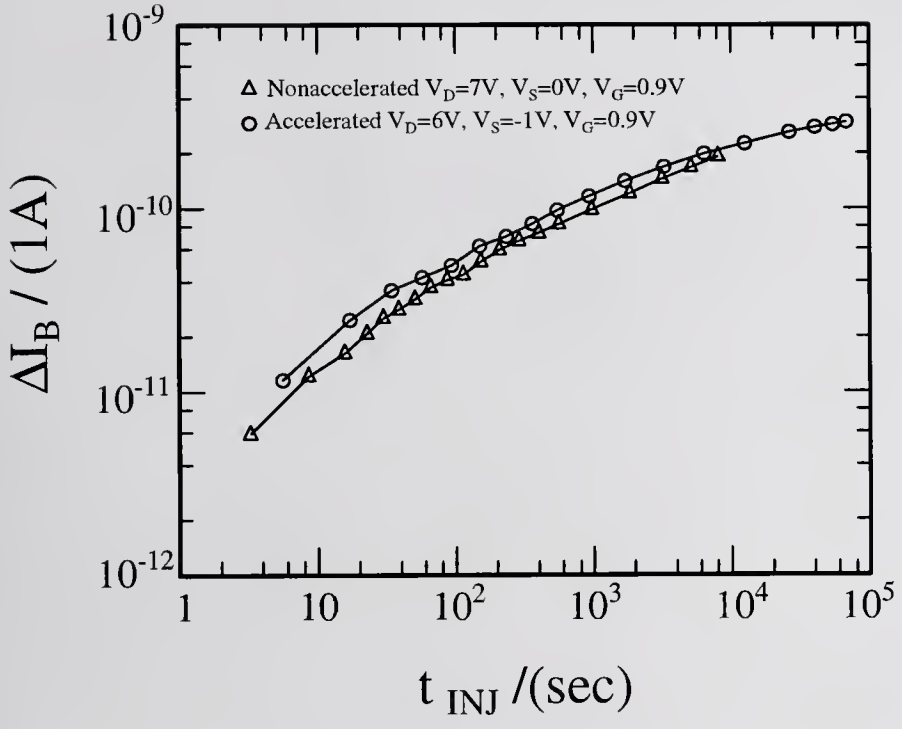



Figure 6.13 Shift in the base current, $I_B$, due to nonaccelerated and top-emitter (source) current accelerated CHE stress.

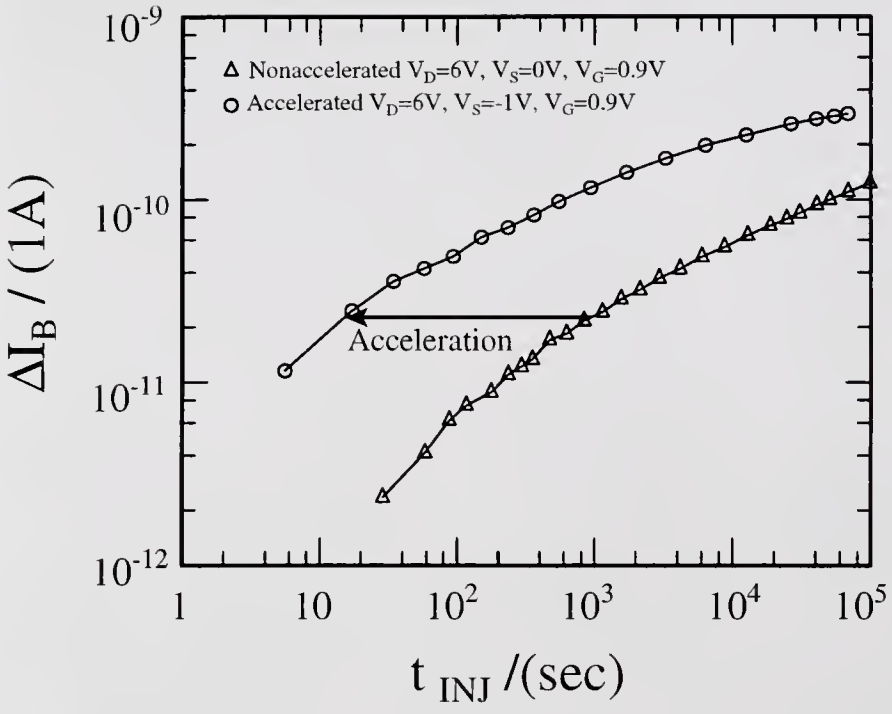



Figure 6.14 Shift in the base current, $I_B$, due to nonaccelerated and top-emitter (source) current accelerated CHE stress at equal $V_D$.

Indeed by comparing this source current-accelerated CHE stress case to the SAM results at $V_{SX}$=0V, $V_{GX}$=0.9V and $V_{DS}$=6V a large acceleration is observed as indicated in Fig.6.14. In addition, proximity of the bottom-emitter junction, which acts as the collector in this forward-biased source configuration, may actually be forward biased near the drain if there is a significant lateral (y-direction) current flowing in the base to cause a lateral base voltage drop. In any case, this current-acceleration scheme is most desirable for the short-channel devices since the limited collection area of the short channel would limit the bottom-emitter acceleration efficiency and the encroachment of the drain and source space-charge regions would reduce the bottom-emitter injected electrons that reach the channel as indicated by the cross-sectional view in Fig.6.3.

A final set of CHE stress measurements were conducted on short-channel (L=1.6μm, W=100μm) nBiMOSTs to illustrate the current-acceleration on $\Delta V_{GT\text{-}sat}$, $\Delta I_{D\text{-}sat}$, $\Delta \mu_{nsat}$, and $\Delta V_{G\text{-}lin}$ since these parameters are directly correlated to the device performance. In addition, a first order correction in $V_{DX}$ was made to compensate for the shift in the threshold voltage, $-\Delta V_{GT}$, due to the forward bias applied on the source/well junction, $V_{SX}$=-0.5V. The results of the CHE stress in the aforementioned parameters are shown in Figs. 6.15-6.18. The nonaccelerated stress was conducted at $V_{SX}$=0V, $V_{GX}$=6.0V and $V_{DX}$=2.0V ($V_{EX}$=0) while the source-emitter current accelerated stress had $V_{SX}$=-0.5V, $V_{GX}$=2.0V and $V_{DX}$=6.2V. It is noted that the degradation in the drain saturation current, $\Delta I_{D\text{-}sat}$, extracted at constant values of $V_D$=$V_G$ (Fig. 6-16) is primarily due to the degradation in the effective saturation mobility, $\Delta \mu_{nsat}$ (Fig. 6-17). An acceleration factor of ~8 is illustrated for $\Delta I_{D\text{-}sat}$, $\Delta \mu_{nsat}$,

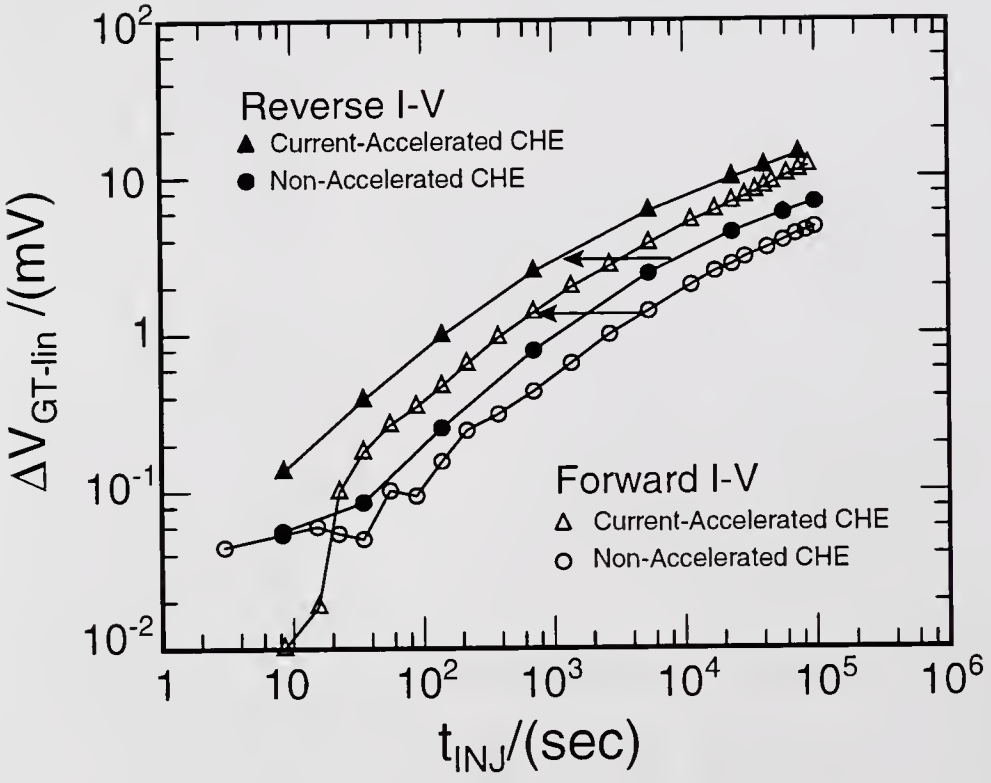



Figure 6.15 Shift in the linear gate voltage characteristics extracted at a constant drain current $I_D$ = 100μA. The forward I-V data is taken with the drain at 0.1V and the source grounded while the reverse I-V data has the source and drain interchanged.

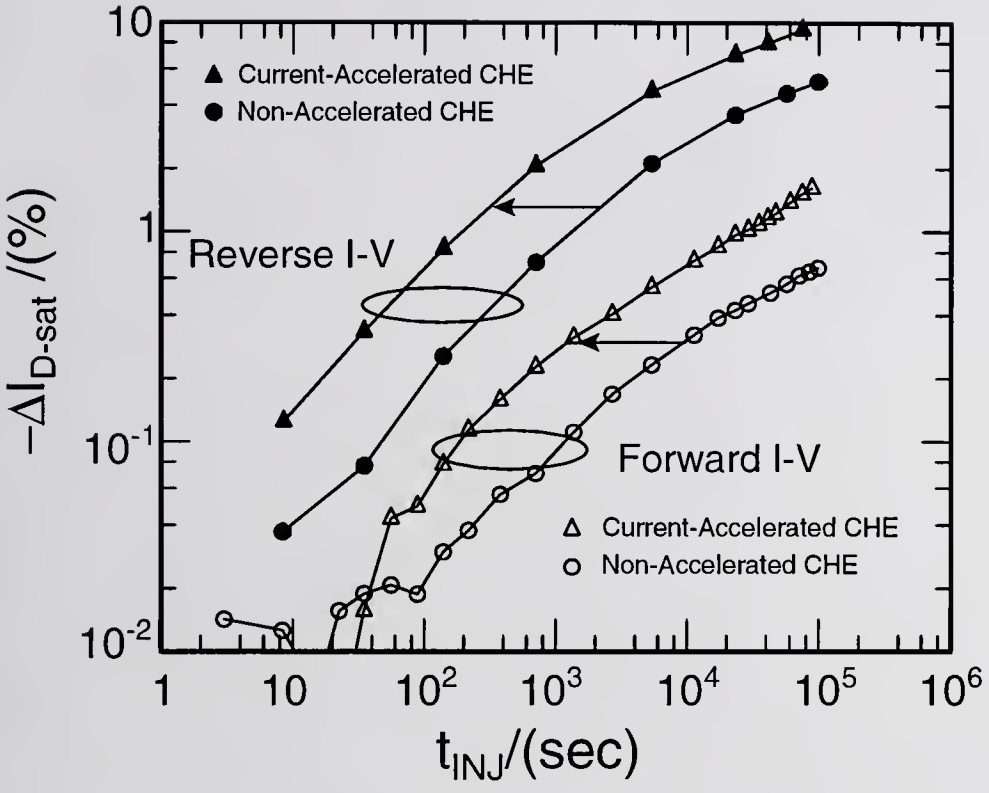



Figure 6.16 Shift in the drain saturation current extracted at a constant value of $V_D = V_G = 0.78V$. The forward I-V data is extracted at $V_D = V_G$ with the source terminal grounded while in the reverse I-V data the source and drain have been interchanged

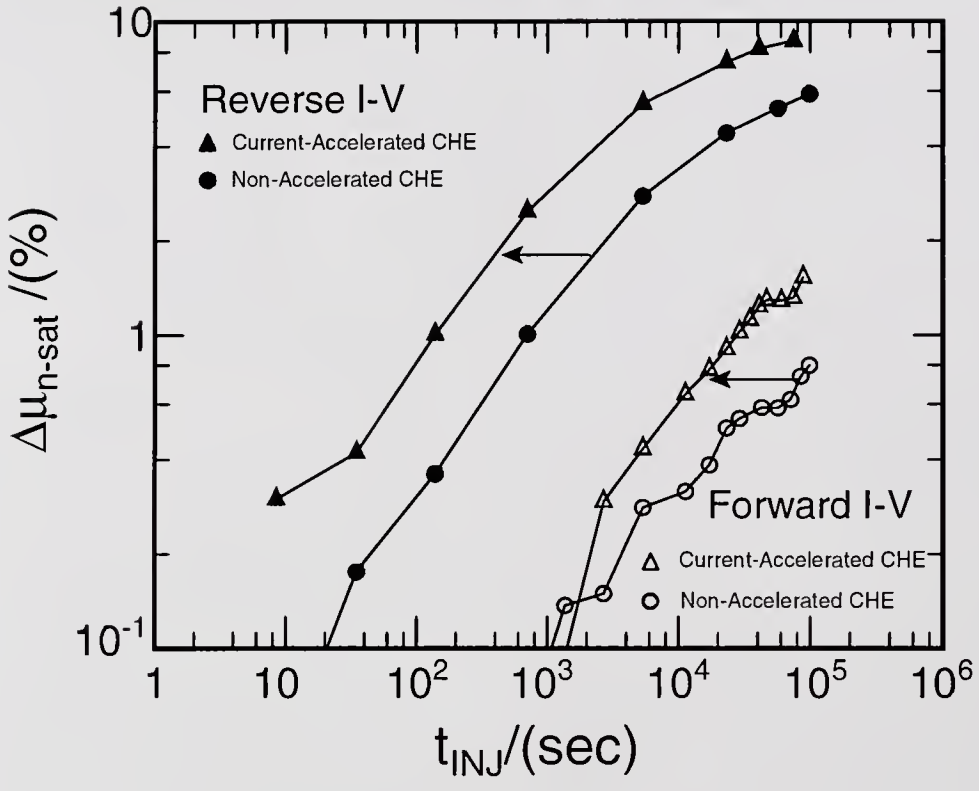



Figure 6.17 Shift in the saturation effective mobility from a fit to the Sah-Pao [55] bulk charge theory. The forward I-V data is extracted at $V_D = V_G$ with the source terminal grounded while in the reverse I-V data the source and drain have been interchanged.

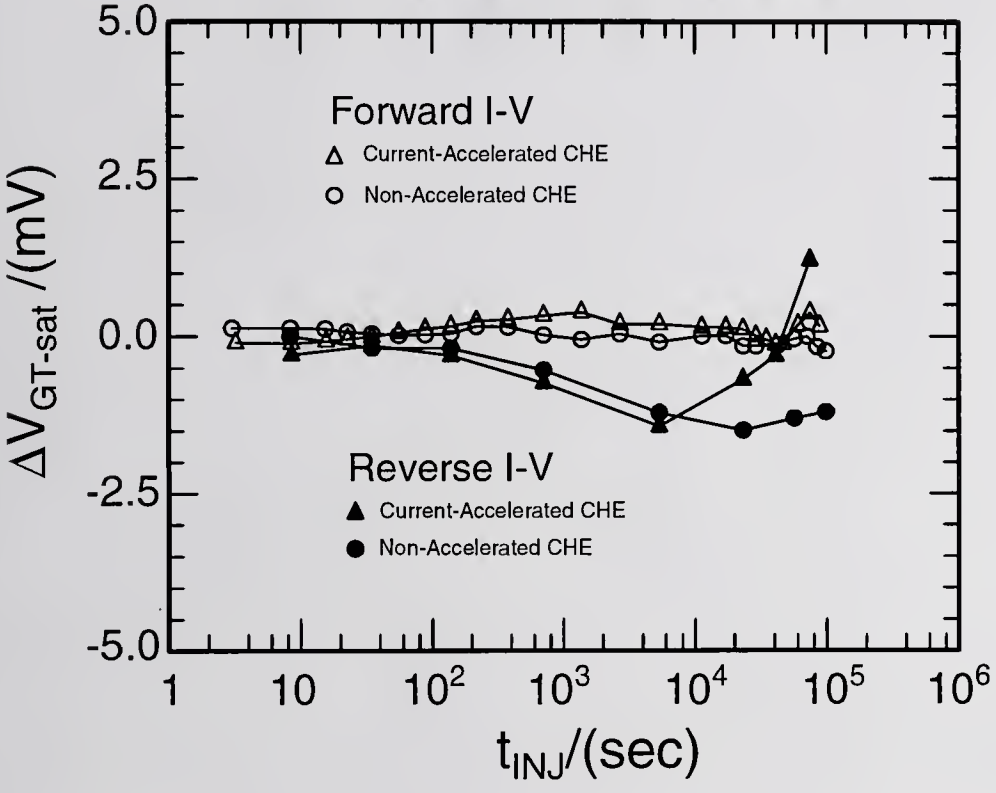



Figure 6.18 Shift in the saturation gate threshold voltage extracted by the Sah-Pao [55] bulk charge theory. The forward I-V data is extracted at $V_D = V_G$ with the source terminal grounded while in the reverse I-V data the source and drain have been interchanged.

and $\Delta V_{G\text{-}lin}$, extracted at $I_D$=100μA, while in contrast the corresponding gate threshold voltage shift, $\Delta V_{GT\text{-}sat}$, extracted in the saturation range was <1mV. The discrepancy between $\Delta V_{GT\text{-}sat}$ and $\Delta V_{G\text{-}lin}$ is due to the fact that the dominant $\Delta\mu_{nsat}$ contribution was factored out of the degradation by the two parameter ($V_{GT\text{-}sat}$, $\mu_{nsat}$) fit of the saturation data to the Sah-Pao theory [55].

# CHAPTER 7
# CONCLUSIONS

Novel measurement techniques and results are obtained in this thesis and described in chapters 2-6. The primary focus of this thesis work is to investigate and model the degradation mechanisms of the current and mobility of the surface-inversion-channel silicon MOS transistor for improving the design methodology of future generations of deep sub-half-micron integrated circuits. Current and mobility degradations in the linear and current-saturation ranges of the MOS transistor current-voltage characteristics are measured under controlled and reversible oxide charging and discharging stress conditions to simulate the electrical stress experienced by MOS transistors during operation. The controlled stresses employed in the stress-and-measure (SAM) experiments of this investigation included: (1) substrate hot electron injection, (2) Fowler-Nordheim electron tunneling injection, and (3) channel hot electron stress. The measurements included: (1) the linear drain current versus gate voltage, $I_D$-$V_G$, (2) the saturation $I_{D\text{-}sat}$-$V_{G\text{-}sat}$, (3) the inversion layer capacitance versus gate voltage, $C_{inv}$-$V_{GX}$, and (4) the base current versus gate voltage, $I_B$-$V_{GB}$, with forward-biased top-emitter or bottom-emitter base current, via the new DCIV method recently invented by Neugroschel and Sah and demonstrated by them and their graduate students.

An in-depth literature review is given in chapter 2. The various physical mechanisms affecting the carrier (electron or hole) mobility in the semiconductor

surface channel investigated by previous authors are described and analyzed or summarized.

Chapter 4 describes the effects of varying the oxide electric field (4MV/cm and 5MV/cm) during SHEi stress on the degradation rate of $\Delta I_{D\text{-}sat}$, $\Delta V_{GT}$, $\Delta\mu_{lin}$, $\Delta\mu_{sat}$, $\Delta S$ and $\Delta I_B$. Two groups of novel experiments were designed to charge (in phase-1) and discharge (in phase-2) the bridging oxygen vacancy among its three charge states +1, 0, −1 in order to give controlled variation of Coulomb scattering of the channel electrons which limits the electron mobility. The results demonstrated reversible degradation in all the aforelisted transistor and material parameters as anticipated by device and material physics. In phase-1 of the SAM experiment, the mobility was observed to decrease during the positive oxide charging ($+Q_{OT}$) by electron impact emission from the $E_C$–7eV level of the neutral oxygen vacancy center, $V_O^0 + e^{-*} \rightarrow V_O^+ + 2e^-$, and it also decreased after negative oxide charging ($-Q_{OT}$) by thermal electron capture at 77°K, $V_O^0 + e^- \rightarrow V_O^-$. In phase-2, the mobility (and also all the other parameters listed above) recovered by low-field SHEi and subsequent thermal capture at the previously positive charged oxygen vacancy, $V_O^+ + e^- \rightarrow V_O^0$. The mobility also recovered by isochronal electric field stimulated electron emission from the negatively charged oxygen vacancy, $V_O^- \rightarrow V_O^0 + e^-$. A novel methodology was demonstrated also in this chapter to separate the $\Delta\mu_{sat}$ and $\Delta V_{GT}$ contributions to the degradation in $I_{D\text{-}sat}$ by using a two-parameter ($\mu_{lin}$ and $V_{GT}$) least-squares fit to the Sah-Pao MOS transistor drain-current equation that included the bulk or body charge [55]. The anticipated linear dependence of the channel electron mobility on the strength (density) of

Coulombic scattering by the oxide charge is demonstrated experimentally in this thesis.

The second part of this thesis, chapter 5, demonstrated a new highly accurate d.c. technique for separating the effects of areal oxide trap nonuniformities in the y-direction (along the channel) and the presence of interface traps on the distortion exhibited in the IV and CV characteristics of a MOST. The technique involved a comparison of the two d.c. measurements: (1) the subthreshold $I_D$-$V_G$ swing and (2) the new DCIV base recombination current, $I_B$-$V_{GB}$. The experiments were conducted in two phases which first generated areally uniform or nonuniform oxide charge $Q_{OT}$ in the gate oxide layer and interface trap $Q_{IT}$ at the $SiO_2$/Si interface. The oxide charge was then neutralized by uniform low-field SHE injection or EFSE emission. The initial positive charging of the neutral oxygen vacancy by electron-impact emission of a bound electron at $E_C - 7eV$ energy level, $V_O^0 + e^{-*} \rightarrow V_O^+ + 2e^-$, was shown to be areally uniform during high-field SHEi ($V_{DS}$=0V) but areally nonuniform during SHEi/CHEi ($V_{DS}$=4V) and FNTEi under accumulation and inversion d.c. gate voltage polarities. The low-field SHEi at 77°K during phase-1 was shown to give nonuniform negative charging of the neutral oxygen vacancy by electron capture into the shallow acceptor level at $E_C - 1eV$, $V_O^0 + e^- \rightarrow V_O^0$. The key assumption made (validated by these experiments) in demonstrating this technique was that any increase in the density of interface traps could not be removed during the uniform neutralization of the trapped oxide charge generated during phase-1.

Finally, a new current-accelerated CHE stress method for rapid time-to-failure extrapolation or determination was demonstrated in chapter 6. The advantages of this

current-acceleration method over the traditional voltage-accelerated CHE stress method is that the new method keeps the kinetic energy and spatial distributions of the channel electrons constant to insure that the same mechanisms are responsible for the change or degradation of the transistor device and materials parameters (listed above). In contrast, the tradition voltage-acceleration CHE method greatly alters both the kinetic energy and spatial distributions of the electrons and hence also changes the fundamental degradation mechanisms during the stress tests. Stress-time acceleration factors of more than 200× are demonstrated for the new current-accelerated CHE stress method in this thesis by forward-biasing the bottom emitter of the n-BiMOST or the source n+/p junction as the top-emitter to increase the flux of electrons flowing through the channel. The saturating behavior of the density of the interface traps generated near the drain, exhibited in the $\Delta I_B$-$t_{stress}$ data, gives for the first time a demonstration of the anticipated asymptotic limit of CHE degradation at lower voltages and long stress times, which degradation clearly cannot increase indefinitely as has been tacitly assumed in the traditional linear or log-log empirical-statistical fit used by manufacturing engineers to develop future generations of deep sub-half-micron silicon MOS integrated circuit technologies.

A major practical application of the new measurement methods and new results demonstrated and presented in this thesis is Reliability Computer-Aided Design (RCAD) for accurate prediction of the reliability of future deep-submicron ULSI technologies under development. This physics-based new RCAD method will provide reliable fundamental degradation rate parameters at the anticipated low operation voltages, so that the RCAD algorithms would not rely on the traditionally used

empirical-parameter extraction procedures to calibrate the CAD tools which is expected to be in serious error due to the saturation or cessation of the fundamental degradation mechanisms and pathways at the low integrated circuit operation voltages (<3.3V to less than 1V) and the corresponding low electron kinetic energies. A major economics impact comes from the more than 100× acceleration of the new current-acceleration method which will shorten the time-to-failure tests for new MOS technologies being developed, from the three-to-six months required in current factory practices to less than 100 hours, thereby substantially speeds up the development and production cycle of new generations of multi-million transistor silicon MOS integrated circuits.

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Jack T. Kavalieros was born in 1967 in Thessaloniki, Greece. He received his bachelor's degree in electrical engineering from the University of Florida with honors in August 1988. He continued his education at the University of Florida under the supervision of Dr. Toshikazu Nishida and completed his M.S. in electrical engineering in May of 1991. His M.S. degree specialization was on the degradation of HCl grown oxides due to forward-biased pulsed electron injection. He then went to work for National Semiconductor in Portland, Maine, during the summer of 1988 under the supervision of Dr. Murray Robinson as part of the semiconductor research corporation (SRC) technology transfer program. He then returned to the University of Florida where he continued his education under the supervision of Dr. Chih-Tang Sah (Ph.D. committee chairman). In the summer of 1994 Jack interned at Intel Corporation under the supervision of Dr. Leo Yau and Dr. Robert Chau, implementing automated wafer-level mobility and channel length measurements. He will be completing his Ph.D. in August 1995 on "The Oxide Charge Degradation of MOS Transistor Current and Mobility in the Linear and Saturation Ranges". He is presently looking to secure a position in the research and development sector of the semiconductory industry.

I certify that I have read this study and that in my opinion it conforms to acceptable standards of scholarly presentation and is fully adequate, in scope and quality, as a dissertation for the degree of Doctor of Philosophy.

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